A Digital Offset Correction Method for High Speed Analog Front-Ends

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***Abstract*—This paper presents an offset voltage correction technique for high-speed digital interfaces. Contrary to conventional way of measuring offset, the proposed technique is based on the phase measurement of a slicer output avoiding the input connection to a common mode voltage. A fully-digital implementation allows phase measurement maintaining offset accuracy. Proper operation of calibration technique is achieved when the input signal is comparable to the offset and sensitivity of the whole interface. Thus, the proposed method could be used during on-line operation, without breaking the communication link. The circuit has been implemented in a 130nm TSMC standard CMOS process, and simulation results show an offset reduction nearly 90% in the analog front-end with a low area overhead.**

***Index Terms*—Offset correction, digital calibration, voltage comparator.**

I. Introduction

In a high-speed serial interface, the front-end of the reception block (Rx) recovers the transmitted information performing three main tasks: equalization, amplification and sampling. After that, the pre-processed signal passes through a Clock-and-Data Recovery (CDR) circuit, which recognizes and separates the clock signal. Besides recovering the clock, the CDR synchronizes the system if the input signal is delivered with a proper quality by previous circuits. The front-end can include a couple of continuous-time linear equalizers (CTLEs), several amplifier stages, a slicer circuit or a sampler as shown Fig. 1 contributing to a large accumulated offset at the slicers input.

The CTLEs offset might saturate the signal at the front of the system making impossible the information recovery. Typically, offset correction techniques are applied in various stages in order to avoid loss of the information. Several offset reduction alternatives have been proposed. In [1], Kimura uses a low-pass RC filter to extract DC of the signal. Kimura [1] calibrates only the analog part by tapping the signal path to sense offset which increases loading. In [2], Redman-White uses a modified CDR to include robustness to offset instead of introducing correction techniques on the analog part of the front-end. The proposed CDR uses ten phases and a complex algorithm in order to extract the input symbols in a way that offset impact is reduced.

This paper presents a solution that reduces offset in high-speed digital interfaces. The reduction technique can calibrate analog and digital part from sampler and can be used to correct the overall offset of the front-end. The correction is performed by sensing the signal phase of the sampler output, generating a control signal with a quite-simple algorithm. The proposed technique works based on the fact that the amplitude of input signal should be less than the offset plus the sensitivity of slicer.

Some advantages of the proposed technique are its low-complexity and fully digital implementation —adding low hardware overhead—. Moreover, offset correction can be applied at any of the stages by sensing only the outputs of the sampler stages. Furthermore, the proposed technique avoids the input connection to a common mode signal as in classical schemes and does not need additional signal paths. The resulting implementation does not compromise high-speed operation and can be used without the need of interrupting data transfer.

II. Proposed Offset Correction Method

Offset correction is typically done in each block of the analog front-end. Fig. 1 shows a classical reception circuit composed by one variable-gain amplifier (VGA), two continuous-time linear equalizer (CTLE), and a 2-tap decision-feedback equalizer using predictive-DFE (prDFE) as its first TAP. For each block an offset sensing and correction circuit is implemented: for the CTLEs is common to use auto-zero; for the comparator is more usual to introduce digital calibration algorithms [3]. In these techniques the offset reduction procedure begins with setting the input signal to a common mode voltage with the purpose of sensing offset only. As a consequence, it is necessary to use auxiliary reception circuits in order to keep the communication link, introducing additional power consumption and area.

The proposed method is shown in Fig. 2, which is based on sensing offset through the comparator (slicer) output signal phase and frequency. This sensing is done by a digital phase detector, whose outputs control the transitions of a Finite-State-Machine (FSM). Then, the FSM outputs are connected to a digital-to-analog converter (DAC), with the purpose of controlling the bias current of the first CTLE. This change in the bias current will induce an additional voltage contrary to the total offset.

When offset if present and its magnitude is too high so that any change of the input signal will not produce any change at the output data, one output of the slicer will remain constant at VDD, and the other will be oscillating for each clock cycle between VDD and ground i.e. from the reset to the comparison phase. As a consequence, the phase detector (PD) —which

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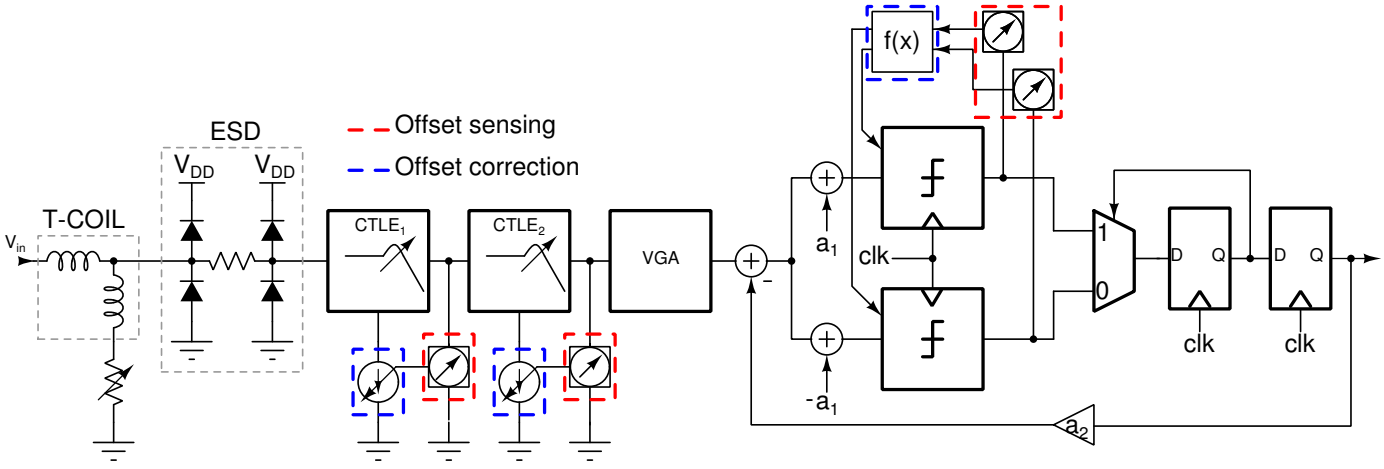

Fig. 1: Classical serial high speed interface with offset correction.

corresponds to a variation of the Bang-Bang circuit (Fig. 3)— senses that one slicer output has a different frequency than the other, producing a change in its UP and DOWN signals. For example, if V_{o1} is stacked to V_{DD} and V_{o2} is oscillating, the PD detects that V_{o2} has a frequency equal to the sampling rate, and that V_{o1} has a lower one; so, the DOWN output is high while the UP signal is low.

These two signals control the FSM transitions regarding the states diagram described in Fig. 4, such that the X_2 signal increases each clock cycle, while X_1 decreases. Then, X_1 and X_2 are converted to analog signals by a digital-to-analog converter, controlling the gate-to-source voltage of transistors M_x and M_y. As a consequence, the circuit modifies the bias current of the first amplifier, trying to compensate the total offset. The calibration finishes when the change in the bias current is able to produce that both V_{o1} and $Vo2$ oscillate between VDD and ground each clock cycle, causing that both phase detector outputs signals are always high.

One of the main advantage of the proposed technique is the fact that the calibration process can be done while the whole interface is still working. It means that, unlike classical offset reduction techniques, the input does not need to be set at a common mode voltage while the calibration is carried out. When offset is larger than the input signal, any change at the input does not produce a variation at the output. If calibration circuit is turned on the offset will be reduce until it is low enough to allow that the input signal can be sensed by the slicer. This characteristic is critical for high speed operation because no additional load is introduced at input of the system. Also, there is no need to execute high complexity algorithms that might introduce latency.

III. Simulation Results

To simulate a more realistic situation, the input of Fig 2 was connected to the output signal of a second-order low-pass programmable filter and a Pseudo-Random Bit Generator PRBS, as Fig. 5 shows. The filter simulates the finite channel bandwidth, while the PRBS acts as the information source. Also, the filter is based on the Gm-C topology, using Nauta circuits [4] as transconductance blocks. The input signal and clock frequency are 3GHz. At this frequency the filter attenuation is 35dB, so its output is 20mV, implying that the offset requirement of the whole system must be less than 5mV. It is important to highlight that all the digital circuits were fully synthesized and simulated at transistor level, allowing to include mismatch and process variations. The CTLE circuits are based on the degenerated common-source topology with resistive load (Fig. 6) which is very common in high-speed applications. The bias topology current is composed by two constant current sources and two additional transistors —M_x and M_Y— used for offset compensation. The comparator corresponds to the strong-arm circuit (Fig. 7) only for validation issues. This topology includes reset transistors at the output nodes for increasing speed [5]. Finally, the current mirrors are biased by the two 8bits R2R calibration DACs.

Figure 8 shows the output signals DAC_1 y DAC_2 of the DAC. Offset was simulated by MonteCarlo analysis in order to include mismatch; however, for explanation purposes, Fig. 8 presents only one iteration. The offset compensation process begins with the two DAC outputs from ground; at this point the comparator can not recover the information from a signal whose amplitude is 100mV. For that reason output signal V_{o2} is always high, while V_{o1} is oscillating between V_{dd} and ground. Some clock cycles later, signal DAC1 increases while signal DAC2 remains constant. After 400ns, these two signals reach a steady-state and the counters and phase detectors are disabled, thus keeping the last data. Once the calibration has been done the two comparator output signals oscillate each clock cycle, recovering the information without breaking the communication link. Moreover, Fig. 9 presents the calibration signals for several Monte Carlo iterations, achieving always a correct offset compensation.

Fig. 11 shows the slicer outputs while an online offset reduction is carried out; in this case, the input signal is provided by the system shown in Fig. 5. At the beginning the signal V_{o2} is always near to V_{DD}, and V_{o1} is oscillating

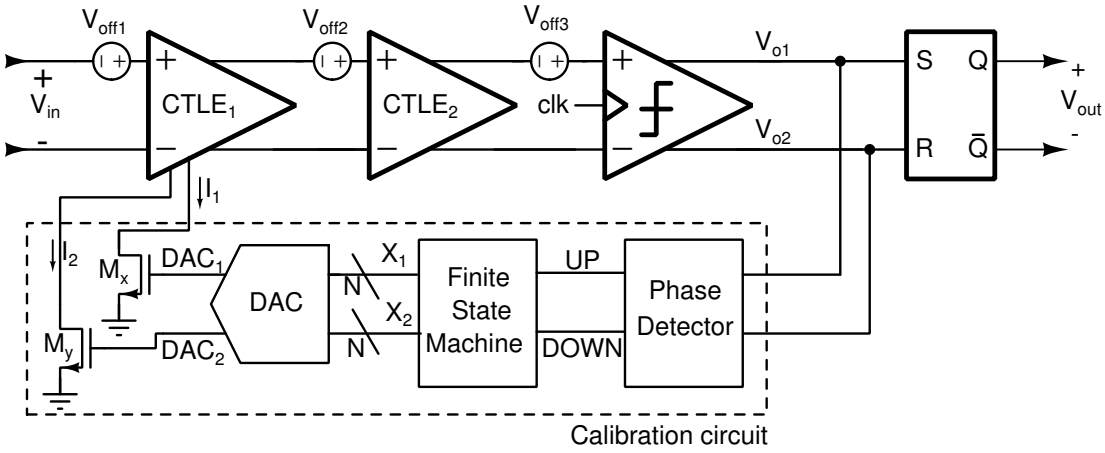

Fig. 2: Proposed offset compensation method.

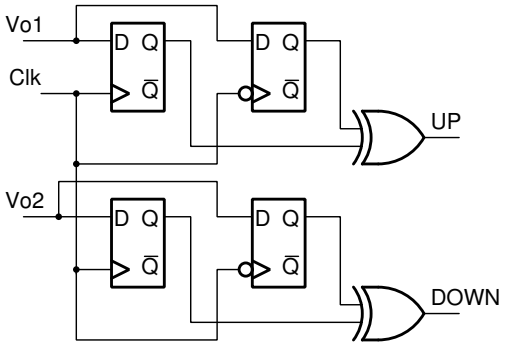

Fig. 3: Implemented Phase Detector.

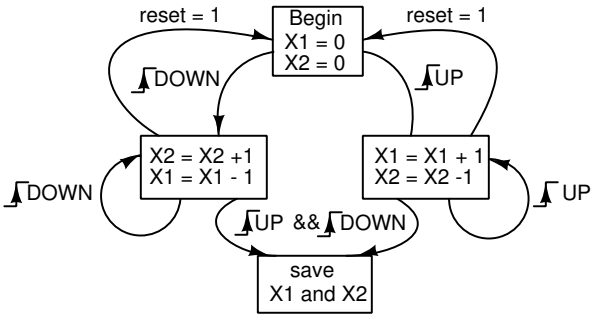

Fig. 4: State diagram of the calibration circuit FSM.

	Typical	Worst Speed Case	Best Speed Case
Offset Before Cal.	100mV	80mV	110mV
Offset After Cal.	220μV	500μV	700μV
Preamp+Comp Power	3.5mW	2.8mW	4.1mW
Additional Power	580μW	430μW	650μW
Supply Voltaje	1.2V	1V	1.4V
Calibration Time	400ns*	400ns*	400ns*

* The clock frequency of the calibration circuit is 250MHz

TABLE I: Performance of the calibration technique

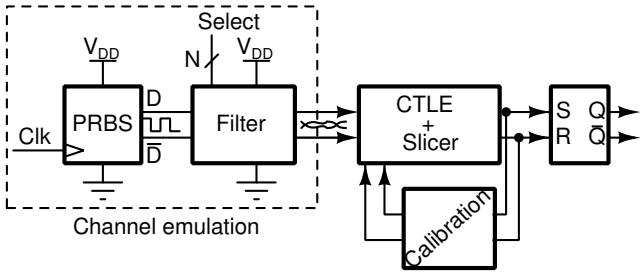

Fig. 5: PRBS and filter used for validating the calibration process.

between the power rails at the clock frequency, indicating that offset is greater than signal amplitude. Then, 400ns later, the calibration circuit adjusts the first CTLE bias current so that both slicer outputs can oscillate regarding the input signal.

In addition, Fig. 10 shows the DAC calibration signals for the worst operation condition: slow process corner, low supply voltage (1V) and low temperature (-40^{o}C); and for the best case: fast process corners, high supply voltage (1.4V) and high temperature (120^{o}C). Both present a successful calibration process in less than 500ns.

Also, table I summarizes the performance of the proposed technique. It is important to highlight that final offset is lower than 1mV, implying a reduction of more than 100X.

IV. Summary

In this paper, a low-hardware overhead calibration technique for high-speed digital interfaces has been proposed. The proposed technique for offset measurement detecs the phase difference between the outputs of the slicer to adjust a bias current to reduce the offset to a permissible value. Calibration is triggered when the amplitude of the input signal at the slicer is less than the sum of the offset and sensitivity. The proposed technique avoids the input connection to a common mode signal enabling the possibility to perform on-line calibration. The calibration circuitry was fully synthesized in 130nm showing the potential to scale the technique to different fabrication process.

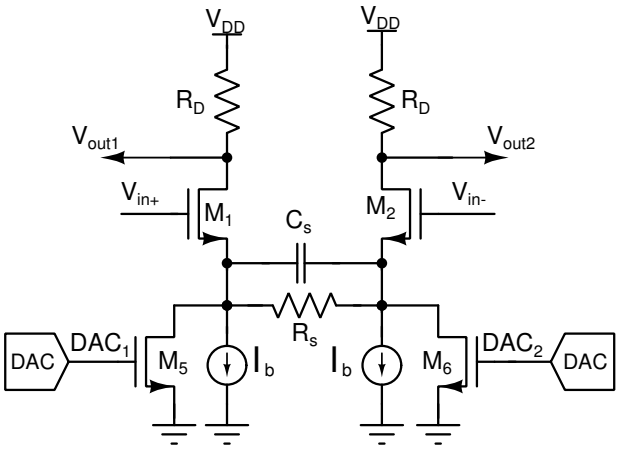

Fig. 6: Traditional Continuous-time Linear Equalizer circuit.

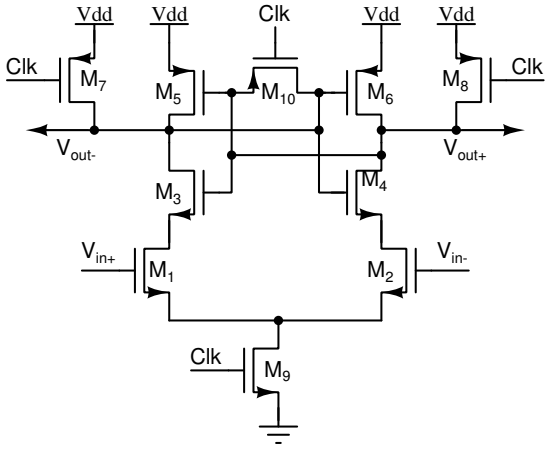

Fig. 7: Strong-arm topology used for the slicer circuit

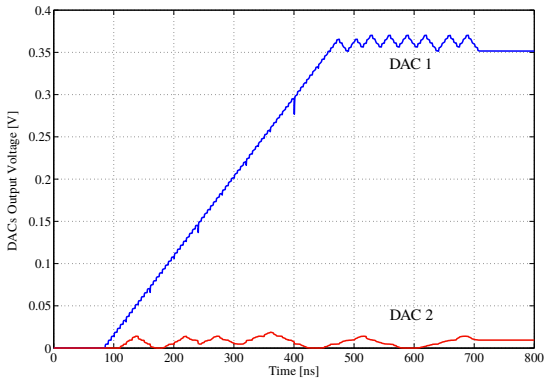

Fig. 8: DACs output signals while the calibration process is carried out.

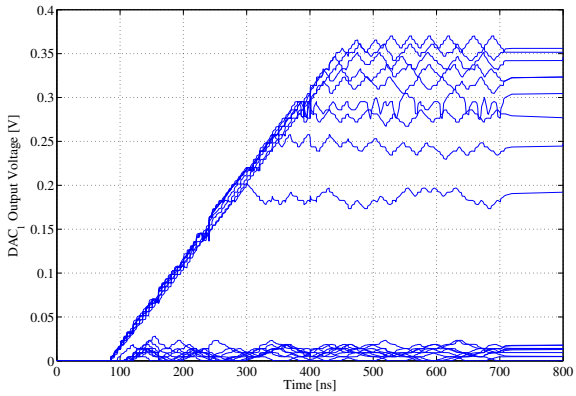

Fig. 9: First DAC output signal for Monte-Carlo samples.

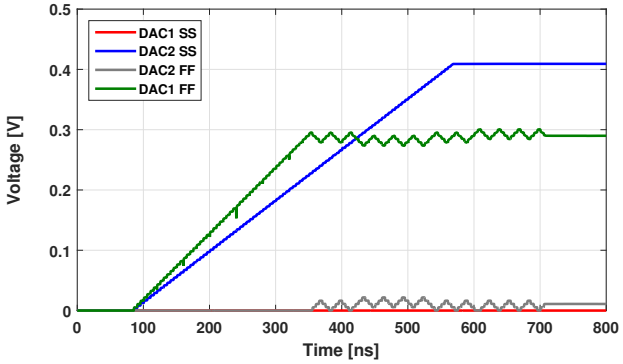

Fig. 10: DACs signals for the best and worst operating case.

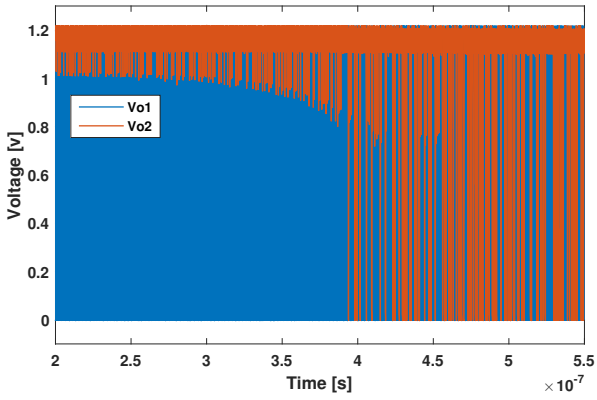

Fig. 11: Comparator output signals while calibration is carried out. The Fig. shows that the system can compensate an offset greater than 100mV.

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