An Offset Reduction Technique for Dynamic Voltage Comparators

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***Abstract*—This paper presents a technique to reduce offset voltage of a dynamic comparator. Contrary to conventional way of measuring offset, the proposed technique is based on phase measurement of comparator output. A full-digital implementation is used to measure phase without impacting offset accuracy. Simulation results show a reduction of more than ten times in the comparator offset with a small increment in power consumption. The technique can be used during normal operation requiring less than 500ns to finish calibration, so that there is not need to break the communication link associated to the comparator. The circuit has been implemented in a 130nm TSMC standard CMOS process.**

***Index Terms*—Offset correction, digital calibration, voltage comparator.**

I. Introduction

The continuous scaling of CMOS technology has allowed the implementation of very-high speed digital interfaces with current data rates above 28Gb/s. At this transfer rate, the channel bandwidth adds losses up to 35dB. Then, the receiver block has to recover clock and data from a signal which amplitude is less than 20mV to prevent the loss of information [1].

To recover the information the receiver block first samples the weak input signal commonly at half transfer rate, and decides if corresponds to a high or low level, similar to an amplification process. If clock is embedded with data, a circuit named Clock-and-Data-Recovery (CDR) extracts clock from the amplified signal and synchronizes the system; as a result the information can be restored. The first step is done by a voltage comparator, which becomes a critical circuit due to specifications such as sensitivity, delay and specially offset. Any change in the offset level can result in a lost of information and can even broke the link.

As a consequence, it is necessary to implement a technique that allows to reduce offset without compromising speed or others specifications. Several alternatives has been proposed by [2] and [4], which include the usage of high-complexity algorithms and digital circuits, adding significant power and area consumption. Moreover, [5] and [6] present two alternatives at circuit level, which add more capacitive load to the comparator and reduce the speed. Also, in all these alternatives it is mandatory to stop the transmission process before calibrating the comparator i.e. a off-line calibration.

This paper presents an alternative technique for reducing the comparator offset, based on the output signal phase. Some advantages of the proposed technique are its low-complexity and fully digital implementation —adding low power and silicon area—. Moreover, it can calibrate the comparator without interrupting data transfer.

II. Proposed Offset Reduction Technique

The proposed technique is based on sensing offset through the output signals phase and transition of a dynamic comparator. This offset measurement is provided by a phase detector, whose output controls the transition of a Finite-State-Machine (FSM) and thus the bias current of a preamplifier, as shown in Fig. 1. The correct adjustment of this currents will reduce the total offset, including extra offset added by the preamplifier.

The system operation can be explained as follows: considering that offset is too high and positive, the output V_{o1} is always equal to VDD, and V_{o2} is continuously oscillating between VDD and ground while the comparator is changing from reset to comparison phase. As a consequence any input signal smaller than the offset level is not able to change the output state, losing the information. Then, the output signals are connected to a phase detector (PD) in order to sense their phase differences and transitions. The PD structure is shown in Fig. 2, which consists of two D-type flip-flops and a XOR gate for each output, similar to a bang-bang phase detector.

Under these conditions, the output DOWN of the phase detector is always low because for each clock cycle the output of the two flip-flops on the right are the same. On the contrary, the UP signal is high because the two left flip-flops output are different for each clock transition. Then, the finite-state machine (FSM) —which basically corresponds to two 8 bits UP/DOWN counters— increases the X_1 output word and decreases X_2. Therefore, the output signal of the first DAC (DAC1) increases, while the second DAC (DAC2) decreases, resulting in a higher bias current I_1 than I_2. This change in the two current sources add an additional offset to the pre-amplifier with the opposite polarity regarding $V_{off1} + V_{off2}$. The calibration finishes when the magnitude of the additional offset is equal to the inherent offset, thus both V_{o1} and $Vo2$ oscillate between VDD and ground each clock cycle, and the phase detector produce outputs are always high.

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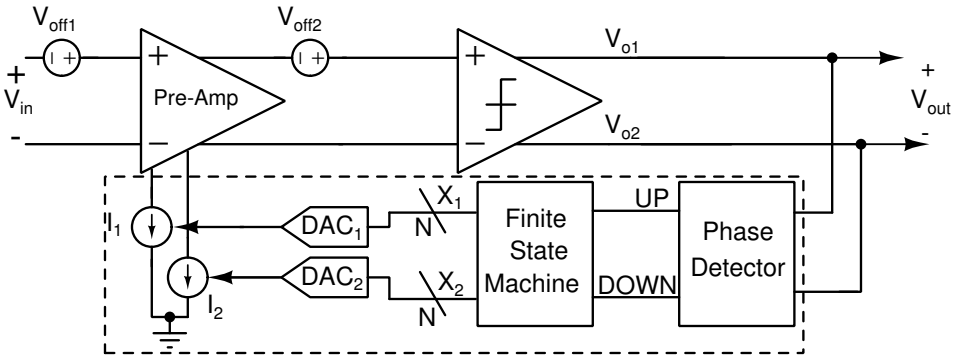

Fig. 1. Proposed offset reduction technique

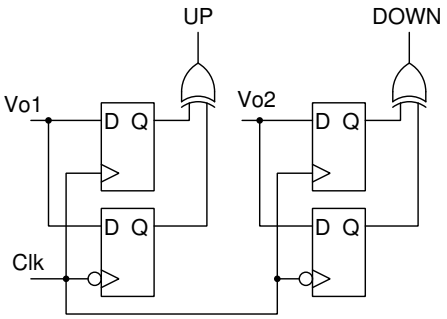

Fig. 2. Phase detector

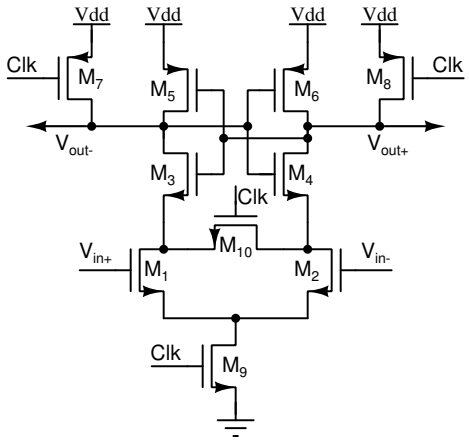

Fig. 3. Strong-arm comparator

One of the main advantage of this technique is the fact that the calibration process can be done while the whole interface is still working. It means that, unlike many offset reduction techniques, the input does not need to be set at common mode level before turn on the calibration. For instance, if the system main core detect a loss of information it can turn on the calibration circuit trying to recover the communication link while reduce offset. While this process is carried out, regardless if the pre-amplifier input signal is the transmitted data or a common-mode level, only one comparator output will be stacked to VDD and the other will oscillating. So, the behavior of the proposed technique will be the same. As a consequence, no additional load is introduced at input of the system so that data transfer speed is not compromised.

In addition, because of the calibration procedure is fully digital, PVT variations and mismatch —including mismatch of the two current sources— have a little effect on the performance.

III. Simulation Results

The circuit simulated using a 3GHz input signal with an amplitude of 20mV, implying that the offset requirement of the whole system must be less than 1mV. It is important to highlight that all the digital circuits were fully synthesized and simulated at transistor level, allowing to include mismatch and process variations.

The comparator is based on the strong-arm topology (Fig. 3), including reset transistors at the output nodes and drain

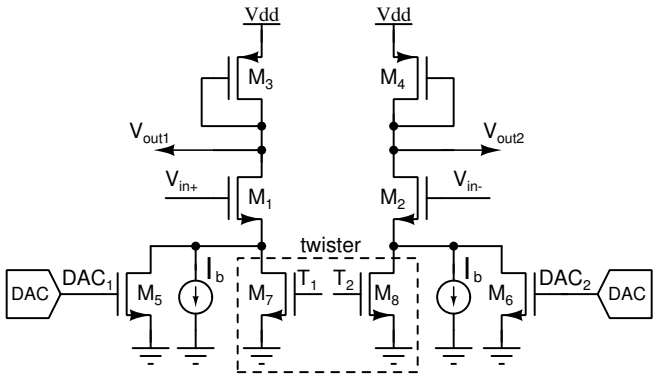

Fig. 4. Preamplifier implemented

of M_1 and M_2 [8]. This circuit was chosen only to show the performance of the proposed technique; however, this method can be used in any other dynamic comparator. Also, the pre-amplifier corresponds to a pseudo-differential pair with a diode-connected transistor as load, and simple current mirrors as tail currents (Fig. 4). It is important to note that the current mirrors are biased by the two 8bits R2R calibration DACs.

Figure 5 shows the output signal of the two digital-to-analog converters DAC1 and DAC2. In this case mismatch was included as offset source using Monte Carlo simulations,

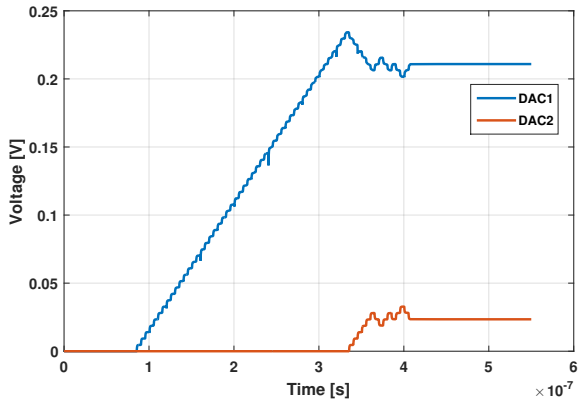

Fig. 5. DACs output signals while the calibration process is carried out

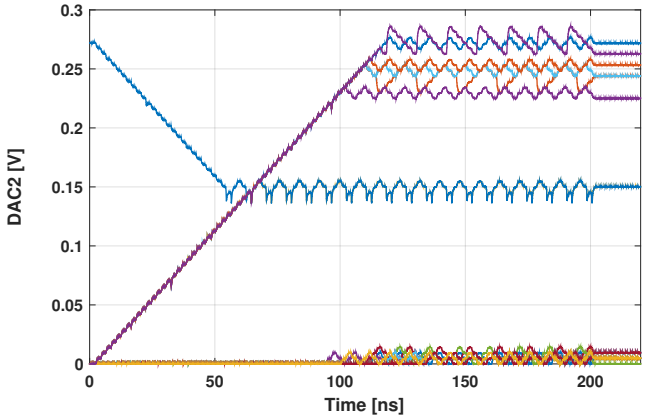

Fig. 6. First DAC output signal for several Monte-Carlo simulations

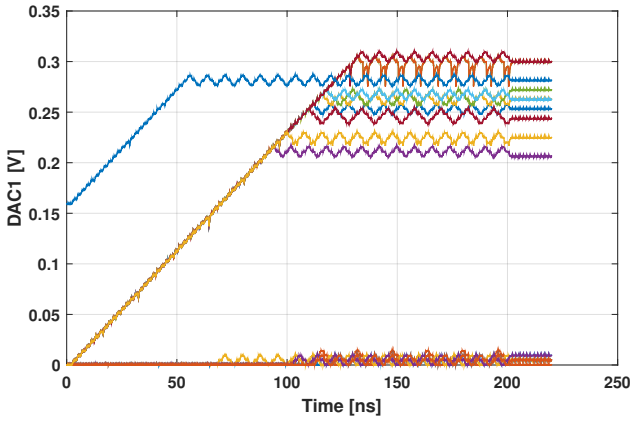

Fig. 7. Second DAC output signal for several Monte-Carlo simulations

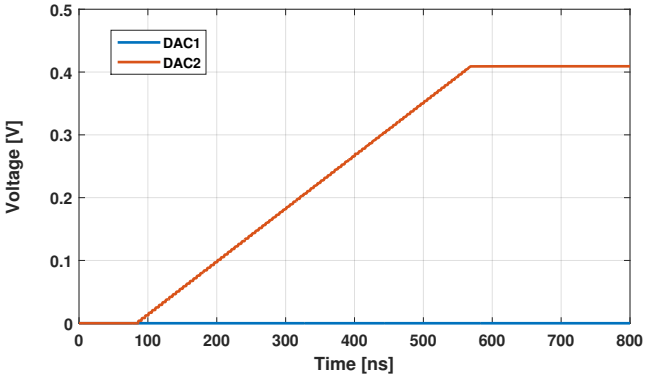

Fig. 8. DACs signals for the worst operating case

and Fig. 5 presents only one iteration. The two outputs start the calibration process from ground; some clock cycles later signal DAC1 increases while DAC2 signal remains constant. After 400ns, these two signals reach a steady-state and the counters and phase detectors are disabled, thus keeping the last data. Once the calibration has been done the two comparator output signals oscillate each clock cycle. Moreover, Figs. 6 and 7 present the calibration signals for several Monte Carlo iterations.

In addition, Fig. 8 shows the DACs calibration signals for the worst operation condition: slow process corner, low supply voltage (1V) and low temperature (-40^{o}C); and Fig. 9 shows the same signals for the best case: fast process corners, high supply voltage (1.4V) and high temperature (120^{o}C). Both Figs. presents a successful calibration process in less than 500ns.

Despite several Monte-Carlo simulations were done aiming to validate the system, and with the purpose of test the proposed technique under extreme conditions, two additional current sources —transistors M_7 and M_8— were added to the pre-amplifier as Fig. 4 shows. As a result, it is possible to produce even more offset. Moreover, signals T_1 and T_2 are produced by two additional DACs so that the additional offset can be controlled precisely. Fig. 10 shows how the calibration can reduce offset while the system is on-line. At the beginning, the comparator can not recover the information from a signal whose amplitude is 150mV. For that reason output signal V_{o2} is always high, while V_{o1} is oscillating between V_{dd} and ground. Once the calibration is turned on and about 100 clock cycles later, the information is recovered without breaking the link. In addition, Fig. 11 shows the calibration signals for this case.

Finally, Fig. 12 presents the layout of the implemented system; its dimensions are 287μm×40μm. The analog circuits

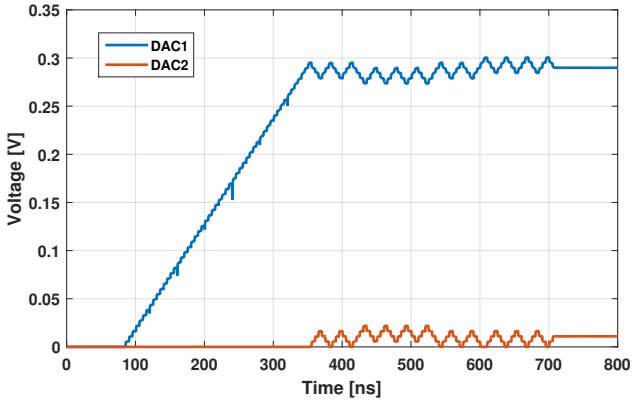

Fig. 9. DACs signals for the best operating case

	Typical	Worst Speed Case	Best Speed Case
Offset Before Cal.	100mV	80mV	110mV
Offset After Cal.	220μV	500μV	700μV
Preamp+Comp Power	3.5mW	2.8mW	4.1mW
Additional Power	580μW	430μW	650μW
Supply Voltaje	1.2V	1V	1.4V
Calibration Time	400ns*	400ns*	400ns*

* The clock frequency of the calibration circuit is 250MHz

TABLE I
PERFORMANCE OF THE CALIBRATION TECHNIQUE

spend more than 50% of the whole area, showing the simplicity of the calibration technique . Also, table I summarizes the performance of the proposed technique. It is important to highlight that final offset is lower than 1mV, implying a reduction of more than 100X.

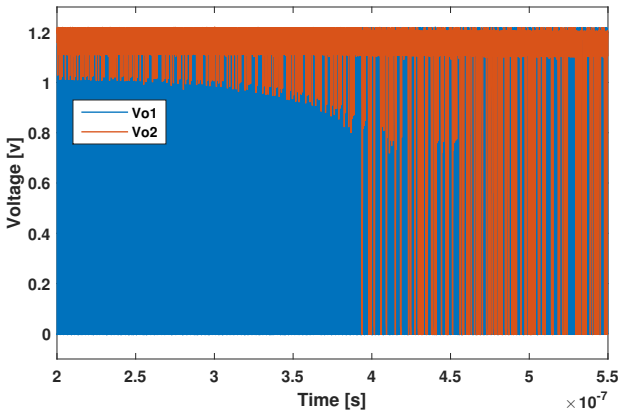

Fig. 10. Comparator output signals while calibration is carried out. The Fig. shows that the system can compensate an offset greater than 150mV

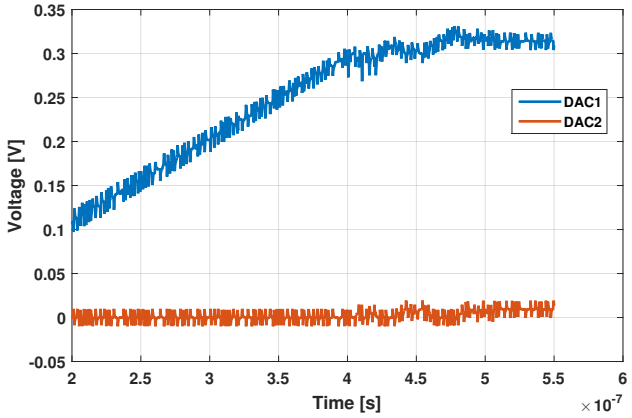

Fig. 11. DACs output signal for the calibration process of Fig. 10

IV. Conclusions

In this paper, a low-cost calibration technique for dynamic comparators has been proposed. The proposed technique uses phase as a variable to measure offset, and adjust a pre-amplifier

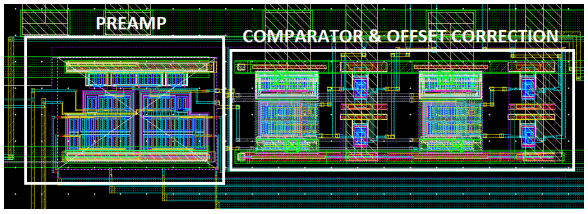

Fig. 12. Layout of the implemented system

bias current to reduce it. The procedure shows a reduction of more than 100x in the circuit offset for worst-speed case. All the calibration circuit was fully synthesized, which allow to extend the technique to different fabrication process and applications.

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