A Compact Industrial-Grade Multi-Threshold Brown-Out Detector

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***Abstract*—This work introduces the smallest reported brown-out detector (BOD) that uses selectable low-power reference voltages, as well as supply voltage division levels, to detect brown-out events at different supply ranges. In contrast to reported BOD architectures, the proposed BOD compensates the low-temperature impact for large impedance branches, particularly at large slewing of ramp-down supply voltages. The circuit was implemented in a 180nm CMOS standard technology allocating an area of 60μm x 100μm including the synthesized logic. Measurement results over voltage and temperature variations show a robust performance within the industrial temperature range from -40°C to 125°C. The BOD draws a typical current of 200nA with five different levels for diverse system-on-a-chip applications.**

I. Introduction

During regular operation of a system-on-a-chip (SoC), it is possible for a disturbance to make the supply voltage fall below a threshold voltage, taking memory and logic away from a well-known state [1]. One of the prevalent causes of a brown-out disturbance is the sudden load increment which a regulator cannot track due to its limited load regulation. In order to prevent unexpected program execution and data corruption in SoCs due to the sudden supply fall or "brown-out," a brown-out detector (BOD) asserts the SoC into reset. Once the supply recovers from the disturbance, the reset signal is released, and the SoC returns to its previous state.

Traditional BOD architectures use two branches feeding a comparator [1]–[3]. A first branch provides a voltage-and-temperature independent voltage reference, and a second branch directly tracks the supply voltage through a voltage-divider V_{div}. V_{div} is intended to be a proportional factor of the monitored supply voltage. In order to obtain low power consumption, the two branches should have a large impedance seen from the supply rails. Consequently, RC constants of the voltage-divider and voltage reference (V_{ref}) are large if branches are biased with currents in the nano-Ampere range to impose low-power consumption. Considering that an under voltage condition or brown-out (BO) is a transient that might have a fast drop and fast recovery, the V_{div} voltage might not be able to track the supply voltage fast enough before the SoC gets into an undesirable state. This issue is relevant at lower temperature operation, regarding the significant lower current. Recent reported BODs at [1]–[3] do not address this issue and even Lee et al., in recent work [4], do not report low-temperature operation.

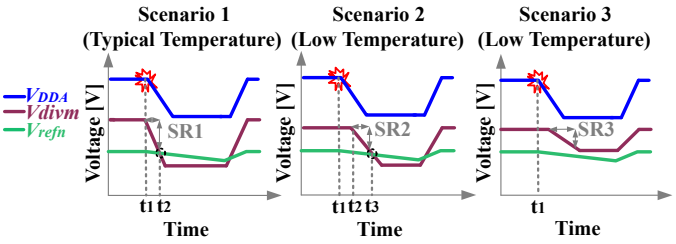

Fig. 1. Low-temperature impact on voltage-divider slew-rate.

Different low-temperature scenarios may lead to different voltage-divider slew-rate values. Hence, in some cases, a brown-out event detection can never take place, as presented in Fig. 1, which displays three different temperature scenarios: a typical temperature case and two others associated with low-temperature. The first scenario illustrates the expected BOD behavior at typical temperature operation when a supply fluctuation occurs at t_1, leading to an intersection at t_2 between the voltage-divider and the voltage reference, resulting in event detection. The same situation occurs in the second scenario for low temperature, where there exists a smaller slew -rate (SR2) than the one presented in the first scenario (SR1) but still, an interception occurs at t_3. However, at t_3 the detection might be late, therefore deciding is required in order to avoid possible data corruption. At lower temperature, a third scenario might exist where the voltage-divider slew-rate (SR3) is smaller than the latter two, preventing the interception, and hence, inhibiting brown-out event detection.

We propose a BOD featuring multiple threshold range levels operating at the industry temperature range from -40°C to 125°C. The BOD compensates the slewing of low power references during low-temperature operation for faster brown-out transitions even at low current bias.

II. BOD topologies

Different circuit topologies can be found in the literature regarding circuit and data protection against supply voltage fluctuations. The BOD alternative presented in [2], is composed by two voltage reference circuits with complementary temperature coefficients, as illustrated in Fig. 2(a). A reset signal will be activated when a complementary to absolute temperature (CTAT) voltage reference stays below a proportional one (PTAT). The main disadvantage of this circuit is that PTAT and CTAT branches are highly dependent on process

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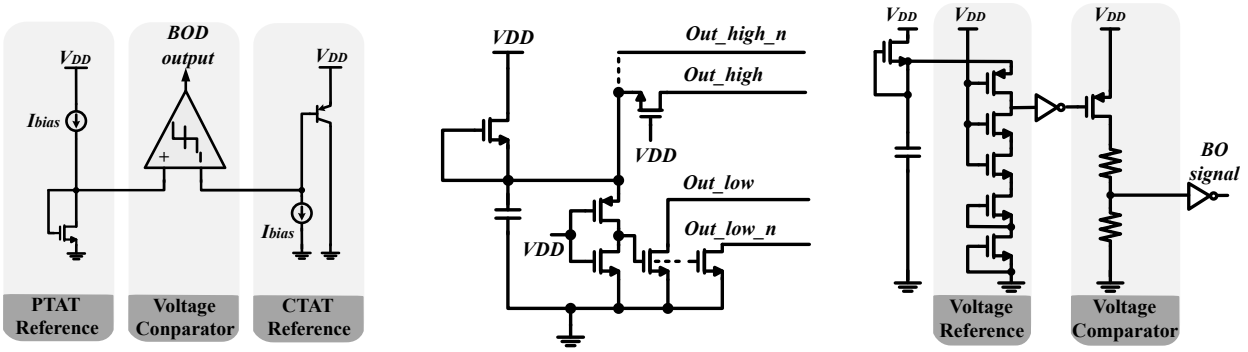

(a) BOD with temperature compensation [2].

(b) BOD for pull-down and pull-up internal POR nodes [5].

(c) Ultra-low DC current consumption BOD [3].

Fig. 2. Relevant reported BOD topologies.

variations. Additionally, large resistors must be added for low power applications penalizing layout area.

Depicted in Fig. 2(b) is the BOD section of the power-on-reset (POR) and BOD architecture proposed in [5]. In this circuit, when a BO event occurs and V_{DD} decreases below the stored voltage in the capacitor (V_{DD} - V_{thn}), the output signals begin to pull-down or pull-up internal nodes in the POR block, enabling a reset mode. Due to the interdependence between the POR and the BO in order to work correctly, and the addition of resistors and capacitors for setting specified voltage values, the circuit increases in complexity and layout area.

A third topology developed by authors in [3] is illustrated in Fig. 2(c) which uses a similar concept as the one presented in Fig. 2(b). After a brown-out event occurs, the inverter input is pulled-up when the supply voltage is one p-type MOS threshold voltage below the stored voltage at the capacitor. Therefore, the voltage comparator is turned on for BO signal activation. Unfortunately, passive resistors and capacitors are highly sensitive to process and temperature variations and occupy larger area on-chip.

Finally, in [1] the adaptive-hysteresis battery voltage supervisor (AHBVS) architecture is presented. The circuit is based on three main blocks: a voltage-divider, a voltage reference and a comparator. Its main purpose is to compare a voltage generated by the divider to the reference one and then take the decision to assert the BOD (reset) signal. The divider output must follow the supply voltage fluctuations to intercept the voltage reference signal.

Low-power references presented at [1], [3], do not include a discussion of results at low-temperature considering leakage current effect that affects considerably circuit performance when subthreshold biasing is used. By simulating the design reported in [1] for the industrial temperature range ($-40°C$ to $125°C$), the effect can be appreciated as presented in Fig. 3. For temperatures below 0°C, the slew-rates of some divider outputs V_{div1} and V_{div3}, are considerably affected. Two undesired scenarios can occur due to the slewing at lower temperatures: the divider output may never cross the reference signal or the interception may occur time afterwards the supply voltage achieves forbidden values. Therefore, some

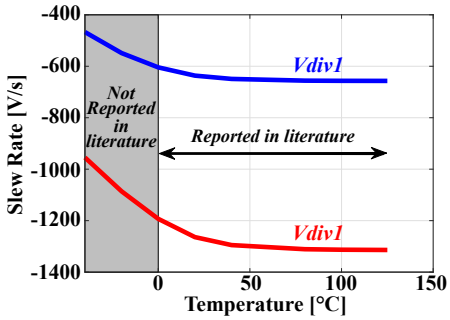

Fig. 3. Slew-rate vs temperature at voltage-divider.

considerations must be taken into account regarding lower temperatures for correct operation.

Two main drawbacks are observed in the relevant reported topologies presented previously: strong temperature dependence and area consumption. Based on these two issues, a programmable threshold BOD with temperature compensated coefficient for low-power applications is presented in the next section.

III. Proposed BOD Architecture

As discussed previously, the reduced temperature range operation, is perhaps, the most limiting factor when trying to achieve a very low-power BOD. As well, although it is one of the most important blocks in the power management unit, its job is very simple: detect when the supply voltage goes under certain voltage threshold. So, one could think that the BOD should be kept as simple as possible. With these two premises, the proposed BOD architecture is presented in Fig. 4. It is composed by three main blocks: a voltage-divider, a voltage reference and a comparator, thought precisely to track and detect variations on the supply, while solving the temperature dependency issue. We employ a native transistor which does not require additional process masks regarding the lack of channel doping. In fact, they are called native transistors considering that they use directly the substrate as channel. Native devices have a lower or zero-threshold voltage

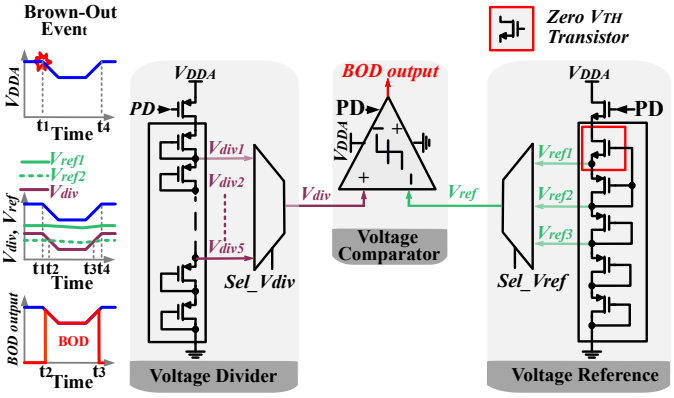

Fig. 4. Proposed BOD block diagram highlighting the proposed voltage divider and voltage reference schemes.

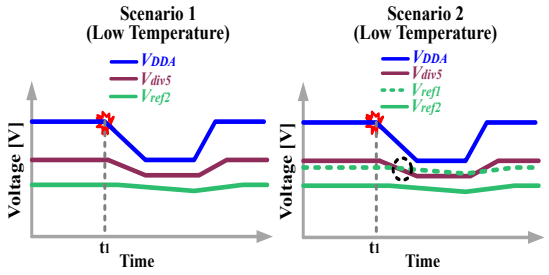

Fig. 5. Low-temperature trimming compensation for brown-out detection.

since the low concentration of charges in the channel requires almost no gate voltage to repel these charges.

In order to solve the effects associated to low-temperature in voltage-divider slew-rate, a trimming circuit is used to compensate the dependencies, to avoid memory data loss. In Fig. 5, scenario 1 precisely illustrates this case, where both voltage-divider (V_{div5}) and voltage reference V_{ref2} curves don't intercept, therefore preventing the possibility to detect the BO event. With the trimming capability proposed in this work, this problem is solved by muxing the voltage reference output with the Sel_Vref signal as illustrated in scenario 2. By activating the V_{ref1} output, the interception between this signal and V_{div5} is now possible, hence, letting the BO detection to take place.

The voltage-divider architecture is composed of a seven stacked 3.3V PMOS transistors connected as diodes, serving as a resistor divider to obtain five different threshold voltage levels. Additionally, a PMOS transistor controlled by the PD signal is used for power-down control.

The reference operation is based on transistor leakage current, achieving moderate precision with low current consumption. The reference voltage values are considered almost constant for more than 50% bias voltage variation. A combination of the NMOS native transistor and regular PMOS transistors allows temperature compensation [4]. However, the number of stacked transistors limits the low-temperature behavior due to the extremely low DC current, that under 0°C is comparable to leakage current. In order to overcome

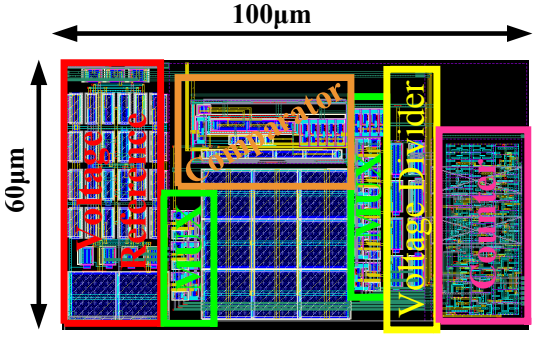

Fig. 6. BOD cell layout view.

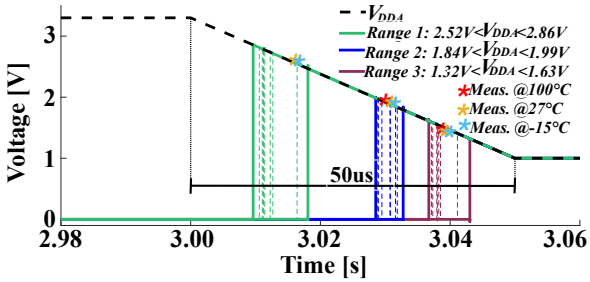

Fig. 7. BOD signal transient measurements and simulations for a supply voltage slew-rate of -46V/s during 50ms and PT variations.

this limitation, a maximum of 4 stacked PMOS transistors and trimming capability are used to accomplish an industry temperature range from -40°C to 125°C. The drawback: higher current consumption (as in the divider).

Given a selected reference level and a voltage-divider level for a specific BO detection range, both signals are compared by a two-stage operational amplifier biased in weak inversion consuming a total current of 10nA. Furthermore, a counter can be connected to the comparator output in order to increase the reset time, to ensure that the voltage supply level has returned to its nominal range after an event detection.

IV. Measurement Results

This section presents measured results of the BOD cell including voltage and temperature variations. A detailed layout view of the designed circuit is shown in Fig. 6, occupying a total area of 100μm x 60μm using a 180nm standard logic technology without additional analog-flavor layers. The reported area includes the counter and additional synthesized digital logic. The BOD is integrated within a full SoC as the trusted supply monitor.

In order to test the functionality of the BOD cell, a brown-out event in the supply voltage (V_{DDA}) —with a slew-rate of -46V/s during 50ms— is used as the test signal. The supply voltage is ramped-down from 3.3V to 1 V, in order to emulate the voltage fluctuation of a low-power system-on-chip that has an always-on domain (AON) and requires to save and protect memory data constantly. Fig. 7 shows a summary of obtained results, low-temperature measurements were performed as low as -15^{o}C and high temperature mea-

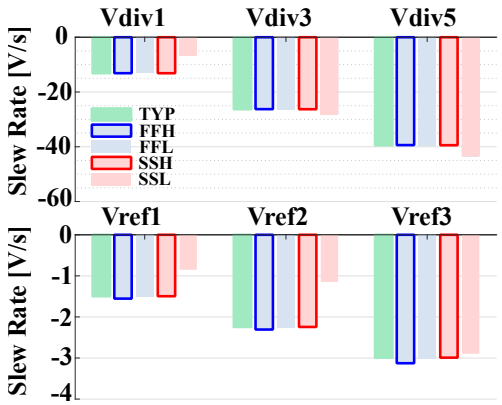

Fig. 8. Slew-rates of the divider (top) and reference (bottom) levels across five relevant corners.

surements as high as 100^{o}C. Indicated results are reported after applying trimming and selecting properly the V_{ref} and V_{div} levels for each BOD range. Although the BOD can be set to have up to five different levels (ranges), only three of them are shown for clarity. Even with proper adjustments, it can be seen variations across PT corners within each detection level due to changes in the ramp-down slopes of V_{ref} and V_{div}. Voltage reference and voltage-divider current consumption depends greatly on the corner, mainly on the temperature. For lower temperatures, current consumption of both blocks are on the order of pico-amperes, while for higher temperatures, the current consumption increases, being even greater than the comparator consumption in the FFH corner (20nA), due to the detriment of the impedance value of the PMOS diode connected transistors.

On the other hand, the reference and divider levels are well behaved in the steady-state over corners, as expected. The problem arises when the BO event occurs, and the supply voltage starts to ramp-down. Shown in Fig. 8, the slew-rates for the reference and divider voltages when the BO event takes place are compared across corners. Measurement results are reported for -15^{o}C, 27^{o}C and 100^{o}C. From this plot the change on the fall-down slopes for low-temperature corners (SSL, mainly) is very noticeable. This undesired behavior is consequence of the low current of the voltage-divider and voltage reference cells at these temperatures, which are not sufficient to discharge (or charge) the input capacitance of the comparator, generating the great changes in the BOD detection levels. As explained previously, this effect was one of the main motivations behind the use of different reference and divider levels, enabling the possibility to compensate the circuit over PT variations, increasing the temperature range of operation compared to the work in [1].

Table I shows a measurement comparison with relevant reported works, as well as a summary of the results. Although the proposed circuit has the highest power consumption among those presented, it is possible to achieve lower power consumption if the lower temperature range is not considered in the operation. For instance, the reported measurements at [1] do not include temperature results below 0°C. Also

TABLE I
MEASUREMENT COMPARISON PERFORMANCE.

	[2]	[5]	[1]	This work
Technology	0.25μm	65nm	180nm	180nm
Supply [V]	2.5	1.1	3.6	3.3
Current [nA]	120	–	**1**	200
$SR_{V_{DDA}}$ [V/s]	–	**-110k to -44**	–	2.3k to -46
Temp. [°C]	–	-25 - 105	0 - 80	**-15 - 125**
# Levels	1	1	1	**5**
Area [mm^2]	–	0.007	0.89	**0.006**‡
Results Summary				
		Min. ∗	**Typ.** ⋆	**Max.** †
Range 1 [V]		2.52 / 2.62	2.75 / 2.65	2.86 / >2.7 ⊎
Range 2 [V]		1.84 / 1.93	1.99 / 1.94	2.0 / 1.97
Range 3 [V]		1.32 / 1.51	1.59 / 1.52	1.63 / 1.54
Current Consumption	Comp. [nA]	3	10	20
	Ref. [nA]	0.1	10	680
	Div. [nA]	0.6	126	3600
	Dig. log. [nA]	0.8	54	300
	Total [nA]	4.5	**200**	4600

∗ Simulation@$-40°C$/Measured@$-15°C$, ⋆ Simulation/Measured@$27°C$, † Simulation@$125°C$/Measured@$100°C$. †Area includes the programmable counter and the additional digital logic. ⊎ Due to test setup limitation, BOD performance was validated until 2.7V.

the proposed BOD allows to select up to 5 different levels while having a low area consumption and robust operation, in comparison to fixed levels at the reported work. Measured operation of the full SoC that contains the BOD demonstrates memory protection for brown out events at low-temperature. These capabilities of the proposed BOD extend its implementation in a broader range of applications.

V. CONCLUSIONS

In this work, we presented a BOD circuit with low-temperature slew compensation for low power applications and multiple BOD levels. Compensated low-temperature effects, especially when the supply voltage starts to ramp-down during a BO event, avoid data loss due to a late or inexistent SoC reset signal. Measured results over PT variations show a robust performance within the industrial temperature range from -40°C to 125°C, with a typical current consumption of 200nA. In comparison to recent research that neglect to consider the low-temperature effects when using large impedance branches, this work achieved a low current consumption even by considering these temperature effects. The proposed multilevel BOD ensures robust operation and broader applicability while consuming the smallest reported area.

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