A Family of Compact Trim-Free CMOS Nano-Ampere Current References

Joan Santamaria, Nestor Cuevas, Luis E. Rueda G., Javier Ardila, and Elkim Roa
Integrated Systems Research Group - OnChip, Universidad Industrial de Santander, Bucaramanga, Colombia.

***Abstract*—This paper introduces a family of three resistor-less low-power, low-area and trim-free current references with low PVT sensitivity. The proposed current sources achieve tens of nano-Ampere current consumption with a temperature coefficient down to 182ppm/°C. The proposed family of current sources are enabled to operate within the 3.3V I/O voltage domain, to avoid additional power consumption from internal regulation, and they are implemented in a 180nm standard logic CMOS process.**

I. Introduction

Emerging powered sensor nodes with low-capacity battery demand nano-Ampere current references to set internal bias current of different always-on circuitry. Current references should operate withstanding a wide temperature range and supply voltage variations without impacting the precision of the circuits they bias. Fig. 1(a) shows a common approach to synthesize a temperature-compensated current source by passing a bandgap voltage reference through a conventional voltage-to-current converter. However, considering the large area required by the resistor, this approach is impractical in area-constrained systems that demand low-power consumption. In addition, this approach needs an error amplifier and a voltage reference, which together may draw significant current and spend additional die area.

Alternatively, current reference circuits add a proportional-to-absolute-temperature (PTAT) current and a complementary-to-absolute-temperature (CTAT) current, as depicted in Fig. 1(b). However, most reported implementations using this principle still require large area resistors to generate PTAT and CTAT currents at the nano-Ampere range [1], [2].

This paper introduces a family of nA current references implemented in a standard logic 180nm CMOS node without additional passive-device layers. Two different principles are used to achieve a resistor-less and opamp-less current reference without incurring in additional post-processing trimming costs. First, generating a source-gate CTAT voltage to compensate the PTAT current dependence of a pull-up pMOS device, as depicted in Fig. 1(c), and using only pMOS transistors to reduce intrinsic process variations. Second, subtracting two PTAT sources using the same pMOS-only structure. The proposed trimming-free family of current references achieves low-temperature sensitivity, drawing currents in the low nA range where leakage models are well behaved by reported accurate foundry models.

II. A Family of Current References

Fig. 1(c) shows the basic principle of using a pMOS transistor as a head current source, where the gate voltage of

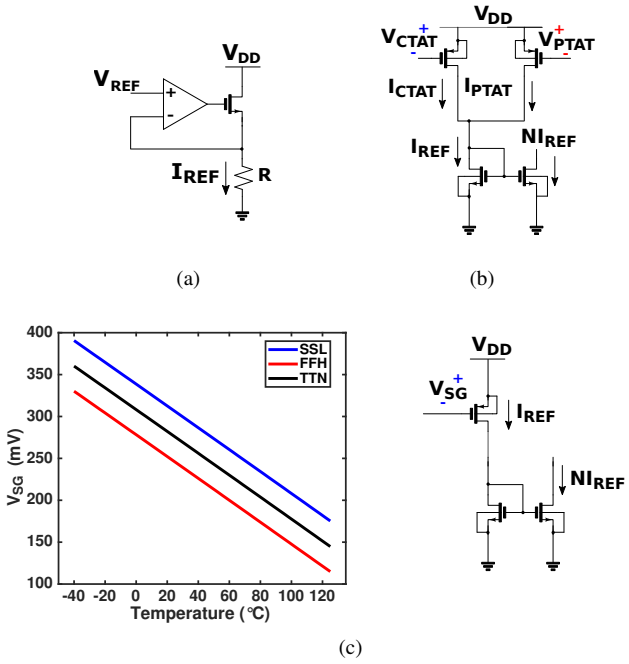


Fig. 1. Traditional approaches to synthesize a current reference: a) voltage-to-current converter-based current source; b) current reference based on the addition of a CTAT and a PTAT current; and c) current source using a pull-up pMOS transistor with V_{SG} CTAT compensation.

the pMOS transistor requires to track V_{DD} in order to avoid supply variations. A PTAT gate voltage or, in other words, a CTAT dependent source-gate voltage is required to compensate the PTAT dependence that exhibits the pMOS source-drain subthreshold current. For instance, the left side of Fig. 1(c) plots the required V_{SG} profile over temperature for a pMOS transistor to obtain a temperature-independent current source of 10nA.[1]

In synthesizing a PTAT voltage, there is a recent trend [2]–[5] to use V_{TH}-based voltage references with transistors operating in subthreshold region, as indicated in Fig. 2. Reported voltage references employ the combination of native devices with regular-V_{TH} transistors (Figs. 2(a) and 2(c)), or the combination of high-V_{TH} with regular V_{TH} devices (Fig. 2(b)), but both cases suffer from process deviations due to the distinctive doping methods. By using only pMOS devices

[1]Corner simulations are reported using the following order: Process nMOS - Process pMOS - Supply Voltage/Temperature; i.e, TTN indicates: Typical nMOS - Typical pMOS - Nominal voltage supply/Nominal temperature, depending on the case.

978-1-7281-0397-6/19/$31.00 ©2019 IEEE

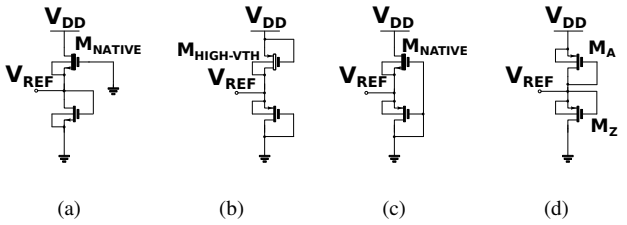


Fig. 2. 2-transistors based voltage references operating in subthreshold.

in a substrate-p process node, as illustrated in Fig. 2(d), it is possible to eliminate the additional and costly post-fabrication trimming steps [3], [4].

Considering that V_{DD} is larger than $6V_T$ and equalizing the subthreshold current of the two transistors of Fig. 2(d), it is possible to express V_{REF} as follows,

$$V_{REF} = mV_T ln\frac{W_A L_Z}{L_A W_Z} + V_{TH_A} - V_{THz} + V_{DD}, \quad (1)$$

where V_T is the thermal voltage, m is the subthreshold slope factor, and V_{TH_A} and V_{THz} are the threshold voltages of M_A and M_Z respectively. If both devices have similar sizes, V_{REF} becomes a PTAT voltage tracking the supply voltage.

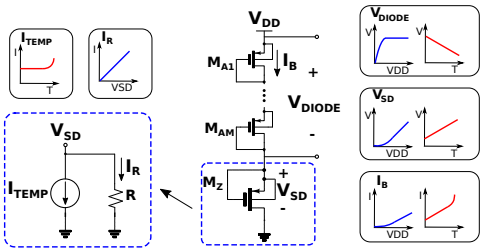


Fig. 3. Behavior of a branch using a transistor with Zero V_{GS} and series diode connected transistors

Most of the work in [3] is based on the expression (1). In contrast, we prove how a series of diodes with an equivalent Norton source, models the subthreshold operation behavior of the circuit in Fig. 3. Regarding the supply voltage dependency, as the voltage drop of the diode-connected transistors remains almost constant, V_{SD} tracks the supply tendency and the I_B current value increases due to the effect of R. The current I_{TEMP} is insensitive to low and medium temperatures, and the parallel resistance R models its dependency on V_{SD}. Fig. 3 also presents the behavior of the equivalent source and depicts that an increment in the temperature causes a decrease in the voltage drop of the diode-connected transistors. Therefore, the voltage on R increases along with the I_B value, presenting a PTAT behavior. In contrast to (1) that indicates that is possible to have CTAT behavior according to the aspect ratio of M_A and M_Z, the model depicted in Fig. 3 indicates an exclusive PTAT behavior.

Following the principle to generate a PTAT voltage, we present three different current references that employ three different proposed techniques to compensate for second-order temperature and supply deviations.

A. Beta-Multiplier Based Current Source

Due to the zero-V_{SG} M_Z transistor, the current across the circuit in Fig. 3 is in the order of picoampere which might be a concern in terms of modelling accuracy or leakage current. To increase the current while keeping reasonable transistor sizes, a beta-multiplier based current source (BMCS), depicted in Fig. 4, avoids the use of zero-V_{SG} transistors.

Considering that a BMCS can generate supply-independent currents, Fig. 4 presents a beta-multiplier based structure to generate a PTAT gate voltage V_G. Start-up circuit is not shown. Since V_P tracks the supply voltage, it is desired that the current across M_P exhibits supply-independence. Thereby expecting that the biasing at M_B does not track the supply voltage.

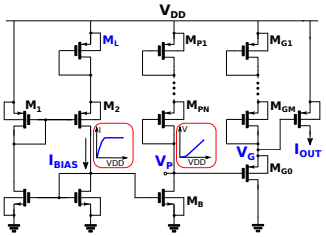


Fig. 4. Beta-multiplier based voltage PTAT generation to generate a current reference.

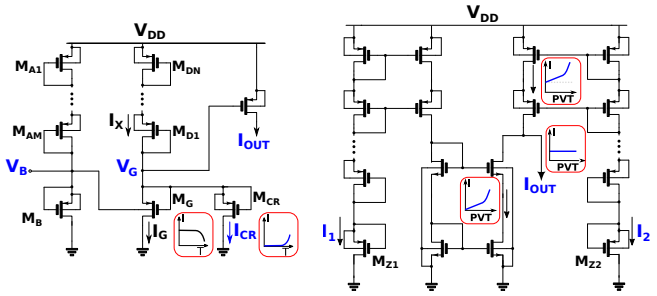
A BMCS biased in weak inversion features a lower supply dependence than strong inversion biased source. The latter might be proved easily, since at weak inversion length modulation depends on the drain-source voltage and thermal-voltage. Considering that the V_{DS} voltages of the transistors in Fig. 4 are larger than the thermal-voltage for a given temperature, branch currents are expected to be insensitive to supply variations, as described by:

$$I_{BIAS} = \mu_P C_{ox} K \frac{W_L}{L_L} n V_T^2 e^{(\frac{-|V_{TH}|}{mV_T})}, \quad (2)$$

where K is associated to the beta gain of the left to right devices ratio in the beta multiplier. In contrast, a beta-multiplier in strong inversion has V_{DD} appearing directly into the current expression due to the channel length modulation effect.

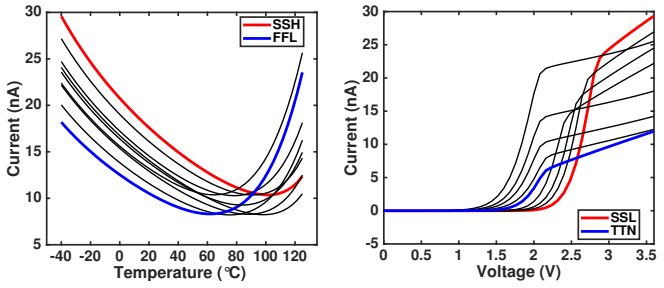
B. High-Temperature Compensated Current Source

Fig. 5(a) shows a proposed high-temperature compensated current source (HTCCS). V_B compensates second-order temperature variations by increasing the body voltage of M_G. As I_X has a PTAT behavior, this strategy increases the V_{TH} of M_G transistor, thus diminishing I_G for achieving the compensation. However, at high temperature, I_X becomes CTAT instead of PTAT and the V_G slope increases. To alleviate this issue, a bleeding transistor M_{CR} is placed in parallel to the V_G node, thus compensating its temperature variation with a high-temperature PTAT current (I_{CR}). The I_{CR} behavior appears because, operating in weak-inversion, the exponential term of the current becomes dominant at high temperatures. The described approach avoids the negative effect of I_G on V_G voltage.



(a) (b)

Fig. 5. Schematics of the proposed a) high-temperature compensated current source (HTCCS), and b) scaled-alike currents subtraction source (SACSS).



(a) (b)

Fig. 6. BMCS output current sensitivity across corners for: a) temperature and b) supply voltage.

C. Scaled-Alike Currents Subtraction Source

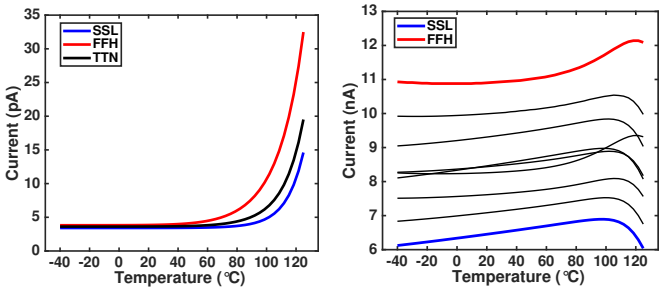
Fig. 5(b) presents a subtraction scheme of two scaled-alike currents (SACSS) using current mirrors from two branches. The proposed SACSS consists of an intuitive scheme to cancel PVT dependence, comprising the subtraction of two scaled currents with alike PVT behavior. Depending on the size of the diode-connected transistors and the number of piled-up devices, the temperature slope and the supply dependence of the current value can be manipulated. With this in mind, and using a different number of stacked diodes in each branch, it is possible to have similar PVT variation slopes and suitable current levels to perform a clean current subtraction.

A good strategy to diminish the supply voltage variations of the SACSS consists of stacking a reduced number of transistors in each branch. This approach also implies a reduction in the minimum supply voltage value needed to obtain a reference behavior in the source. However, as the number of diodes decreases, the current levels of these branches become closer and the subtraction produces a lower output current value. The latter effect can be countered by using a current mirror with such a copy rate to produce the desired output current value.

III. Performance Results

We performed corners and Monte Carlo simulations in order to validate the proposed circuits. Fig. 6(a) shows the output current across corners for the BMCS. The results expose a moderate process dependence behavior all along the temperature range. The maximum variation occurs at high temperatures, where the current variation across corners can reach 16nA. Fig. 6(b) reveals a strong dependence of the BMCS regarding the supply voltage. The observed variations appear due to, referring to Fig. 4, the increase of the current value in M_B transistor. This change is caused because V_P tracks V_{DD}, showing alike I_{DS} vs V_{DS} characteristic. The current increment also produces an alteration in the diode-connected transistors voltage, thus preventing V_P from following V_{DD} accurately. Hence, the nominal voltage for proper operation ranges is between 2V and 3.6V.

The HTCCS presents the PTAT behavior correction performed by the bleeding transistor M_{CR} as Fig. 7(a) reports. Fig. 7(b) depicts the output current of the HTCCS across corners. These results reveal low sensitivity against PVT variations all along the industrial temperature range. The results indicate a maximum current gap of about 6nA, which is caused by the extreme corners: FFH and SSL.

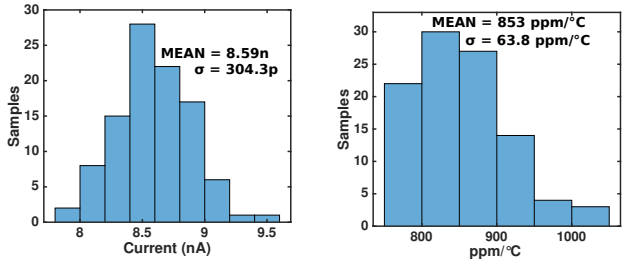


(a) (b)

Fig. 7. a) Compensation current across bleeding transistor, b) HTCCS output current across corners.

Fig. 8 summarizes the Monte Carlo simulations applied to the HTCCS. Fig. 8(a) reports a mean output current value of 8.6nA with a standard deviation of about 4%. Fig 8(b) shows an output current deviation between 750 and 950ppm/°C, for more than 90% of the analyzed points.

Fig. 9 shows the results of a PVT variations analysis applied to the SACSS source. The output current behavior (Fig. 9(a)) discloses very low output current value fluctuations within the analyzed temperature range. The maximum appreciated difference between current values is of, roughly, 0.3nA. Fig. 9(b) illustrates the output current dependence on the supply voltage. Unlike the BMCS, the SACSS delivers an output current along a larger voltage range. Furthermore, low supply



(a) (b)

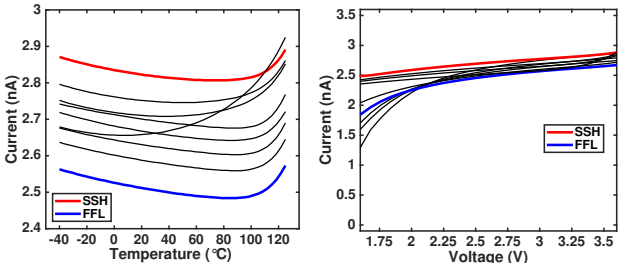
Fig. 8. Monte Carlo simulation results for the HTCCS.

TABLE I
PERFORMANCE COMPARISON

Parameter	This work*			[5]*	[2]**	[6]*	[7]**	[4]**
	BMCS	HTCCS	SACSS					
Output current (nA)	8.28 – 29.5	6.03 – 12.14	2.48 – 2.92	0.005	6.4 – 6.8†	91 – 96†	5 – 12†	31 – 36.5†
Current Consumption (nA)	12.3	0.14	13	0.029	7.75	450	68.1	0.68
Temp. Range (°C)	-40 – 125	-40 – 125	-40 – 125	0 – 100	0 – 110	-20 – 100	-20 – 80	-40 – 120
Temp. Coefficient (ppm/°C)‡	8040	430	182	31	283	288	1190	282
Area (μm^2)	1114	450	9268	N/A	55000	N/A	120000	16878

*Simulated results. **Measured results. †Estimated from reported results. ‡ Temp. Coefficient (TC)= $10^6 * (I_{max} - I_{min})/(I_{nom} * (T_{max} - T_{min}))$

sensitivity is achieved for supply voltages from 2V and above, where the output current presents a maximum variation of about 0.4nA.

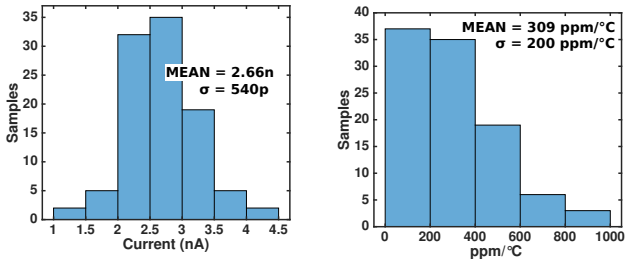


(a) (b)

Fig. 9. SACSS output current across corners for: a) temperature and b) supply voltage sweep.

Fig. 10 displays two histograms for the output current of the SACSS, obtained through the use of Monte Carlo analysis. In Fig. 10(a), the results show a mean current value of 2.7nA, along with a standard deviation of roughly 20%. These calculations allow concluding that the SACSS presents an acceptable output current regarding random variations and taking into account the nano-Ampere magnitude order of the current reference. 10(b), reports an output current deviation between 0 and 600ppm/°C, for more than 90% of the analyzed points. This evidences an improvement in the robustness against random variations in comparison to the HTCCS.

Finally, Table I summarizes the comparison results between the three proposed nA current references and previous works. In this work, the best current reference, regarding current consumption, corresponds to the HTCCS. However, the temperature coefficient (TC) can reach 430ppm/°C. The work reported in [5] seems to be the best concerning total current consumption and output current, but the TC is reported only from 0°C to 100 °C instead of the industrial range from -40°C to 125°C. The SACSS presents the lowest variation among the current sources family proposed in this work, the variation of 182 ppm/°C competes with [2], [4], [6], while generating lower output currents. Although the BMCS reports the worst variation with respect to the other works, its low-area enables to apply it in multiple places within a SoC employed



(a) (b)

Fig. 10. Monte Carlo simulation results for the SACSS.

for applications with defined environmental conditions.

IV. CONCLUSION

A family of three new current references with competitive PVT sensitivity was presented. Monte Carlo results were also included. Among the proposed current sources, a TC up to 182ppm/°C can be achieved with tens of nano-Ampere current consumption. As well, with the proposed approach, this paper exposes an area improvement in contrast with prior works, accomplishing 450μm^2 as the best. The proposed current references were implemented in a 180nm digital CMOS process node without additional passive-device layers.

REFERENCES

[1] B. Yang *et al.*, "An Accurate Current Reference using Temperature and Process Compensation Current Mirror," *A-ASSCC*, 2009.

[2] Y. Ji *et al.*, "A 9.3nW All-in-One Bandgap Voltage and Current reference circuit," *ISSCC*, 2017.

[3] Q. Dong *et al.*, "A 114-pW PMOS-only, Trim-Free Voltage Reference with 0.26% within-Wafer Inaccuracy for nW Systems," *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, 2016.

[4] Q. Dong *et al.*, "A 1.02nW PMOS-Only, Trim-Free Current Reference with 282ppm/°C from -40°C to 120°C and 1.6% within-Wafer Inaccuracy," *ESSCIRC*, 2017.

[5] H. Wang and P. P. Mercier, "A 14.5 pW, 31 ppm/°c Resistor-Less 5 pA Current Reference Employing A Self-Regulated Push-Pull Voltage Reference Generator," *ISCAS*, 2016.

[6] Osaki *et al.*, "Nano-Ampere CMOS Current Reference with Little Temperature Dependence Using Small Offset Voltage," *MWSCAS*, 2010.

[7] "A Nano-Ampere Current Reference Circuit and its Temperature Dependence Control by using Temperature Characteristics of Carrier Mobilities," *ESSCIRC*, 2010.