# On UVM Reliability in Mixed-Signal Verification

Wilmer Ramirez, Hector Gomez and Elkim Roa
Integrated Systems Research Group OnChip, Universidad Industrial de Santander, Bucaramanga, Colombia
{wilmer.ramirez,hector.gomez}@correo.uis.edu.co, efroa@uis.edu.co

***Abstract*—During the last decade, Universal Verification Methodology (UVM) has become a popular standard test methodology for verification of intellectual property (VIP) within digital and mixed-signal systems. UVM prominent features include stimulus automation, I/O checking and code reuse. This paper analyzes the strengths and weaknesses of UVM along with measurements of reliability using a 32-bit LPDDR3 memory interface and a bandgap voltage reference. Simulation results indicate that reliability is limited by complexity of the circuit under test and proper UVM setup to get considerable analog simulation coverage. For analog cases, UVM-AMS can render low reliability considering that a common practice in analog design is creating multiple testbenches according to the function/domain tested. VIP by itself should be used as a complement to traditional verification practices even when assuming access to a fully detailed UVM-AMS VIP.**

***Index Terms*—System-On-a-chip, Verification IP, UVM, mixed-signal**

## I. Introduction

The semiconductor industry developed the Universal Verification Methodology (UVM) as a proposal to offer reliability, reusability, and robustness to functional verification of system-on-a-chip (SoC) design blocks. Considering its wide adoption, UVM quickly became an IEEE standard [1]. UVM applies object-oriented programming properties that allow for the creation of dynamic objects in order to design modular testbenches easily configurable to verify multiple functionalities either by running automated tests in series or in parallel [2]. Hence, UVM helps optimize verification time, avoids manual intervention by the designer during test execution, and allows code reuse [3] [4]. In contrast, traditional verification uses static objects from Verilog/SystemVerilog that present little modularity restricting code reuse. Another drawback of traditional functional verification is the lack of structured tools to test complex systems with multiple ports and functionalities, causing simulation to become a tedious and unreliable process. Although UVM has become popular for digital system verification, there is no community consensus on UVM effectiveness on mixed-signal systems verification, and an analysis of its reliability is still missing considering its application.

The effectiveness of UVM depends on the design under test. We proved that for an LPDDR3 memory interface test, UVM coverage is limited by current commercial tools considering data size. On the other hand, UVM for mixed-signal (UVM-AMS) might not be efficient to check when compared to pure analog functional verification tools. In cases where most specifications are associated with analog/continuous data, coverage efficiency is limited for UVM-AMS. UVM usage for analog systems can be seen as a type of analysis that is behavioral instead of a quantitative measurement process.

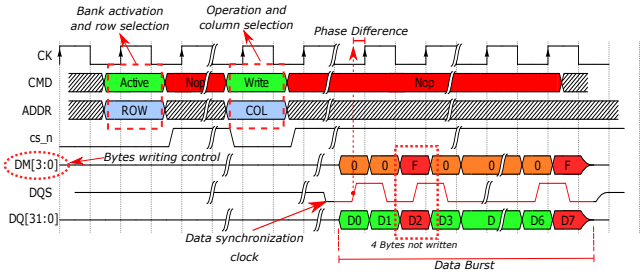


Fig. 1. LPDDR3 data transferring protocol.

A key contribution of this work is the presentation of an analysis with performance measurements of how reliable UVM-AMS is in functional verification. Two different systems are presented as instances, and for each of them a verification system using UVM is presented in order to prove how effective/sufficient are the given tests. This paper seeks, through particular examples, to reach general conclusions about the effectiveness of UVM-AMS as a verification methodology for complex and simple systems.

## II. VIP Systems Implementations for Digital and Mixed-Signal Circuits

A UVM-based VIP presents the execution sequence showed in Fig.2. A list of test sequences is executed sequentially or in parallel, where stimuli are transported to the BFM to excite the DUT. The DUT response is observed and analyzed automatically to ensure the correct behavior of the design. Two different designs are tested by UVM-based VIPs in order to verify UVM-reliability in functional verification for each design. A description of the tested designs along with a description of the implemented UVM-based VIPs and their simulation results for each of them are presented.

### A. A 32-bit LPDDR3 Memory Interface VIP

*1) Design:* Low-Power DDR (LPDDR) memories are dynamic RAMs that work at double data rate since they use both clock edges to transfer data. These memories are characterized by their low power consumption compared to DDR. The system worked in this section is a 32-bit mobile low-power DDR3 with 4Gb synchronous dynamic random-access memory, which is internally configured as an 8-bank DRAM and clocked at 800MHz. The LPDDR3 operation modes of data transfer are described in Table I.

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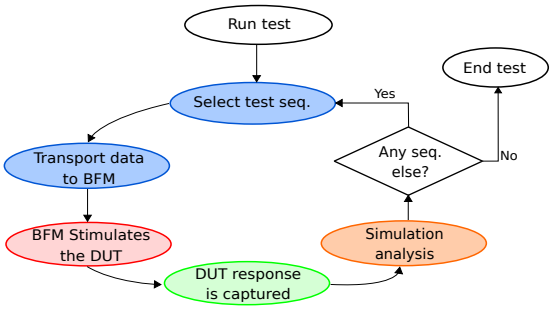


Fig. 2. Execution steps of a UVM-based VIP .

TABLE I
LPDDR3 DATA TRANSFER OPERATION MODES.

| Operation Mode | Characteristics |
|---|---|
| Active | This mode activates a selected memory bank in order to perform an operation on the same bank. |
| Writing & Reading | The write and read bursts are performed in their respective operation mode. To access to any of these modes, the LPDDR3 must pass by the Active mode first. |
| Precharge | If a bank is already active, the LPDDR3 must pass by this mode before operating the bank. |

Performing data transactions with these memories requires to follow the protocol described in JESD209-3 [5]. Fig.1 illustrates the protocol to transfer a data burst (8 length) to the memory using a write operation. The process is performed in steps, first activating the memory bank and the row to operate; and then, the operation to be performed and the column to be operated is selected. Once this is done, the transfer of the 32-bit data burst to or from the memory begins with the selected address (bank, row and column), and the next seven directions of the data burst are the next seven columns. All the steps are separated by times established by the protocol. In the write operation, it is possible to select which bytes of a 32-bit data are written. In the read operation, the process is similar but in this case, the byte-writing control signal does not intervene, and the data strobe is in phase with the clock. More details about the LPDDR3 operation can be found in [5].

*2) VIP implementation system:* The VIP adapts the memory interface to play the role of bus functional model (BFM) in the verification system. A provided memory model is used as DUT and in this way, the VIP can verify the correct communication process through the memory interface operating as BFM. Fig.3 shows the state machine implemented for the memory interface (adapted as BFM) to perform transactions to memory model depending on the requirements of the VIP system in the course of the verification. The wrapped made to indirectly test the LPDDR3 memory interface is illustrated in Fig.4, where write-and-read sequence items are transported to the LPDDR3 virtual interface to perform both operations in the memory using a pseudo-random address, a pseudo-random data, and a pseudo-random Data Mask (DM) activation for whatever of the eight 32-bit data in the burst for the write operation. A

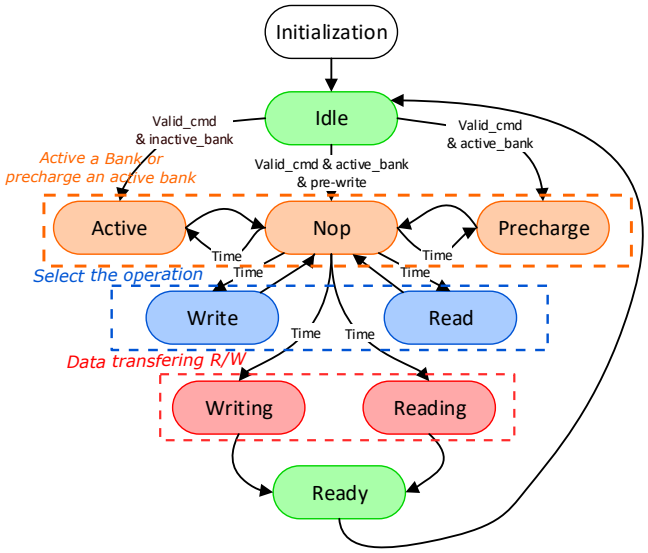


Fig. 3. State machine of the memory interface adapted as BFM.

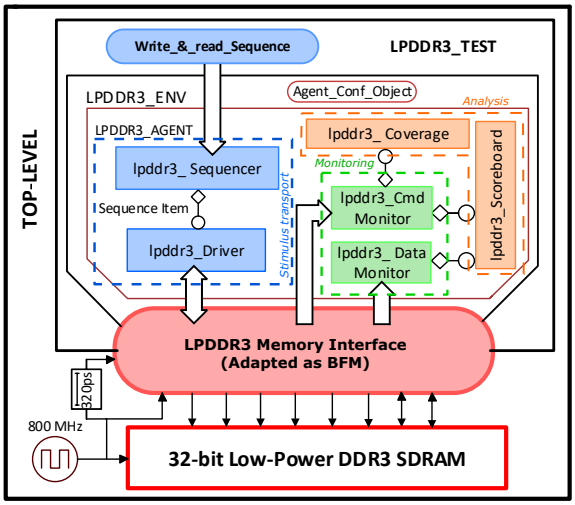


Fig. 4. UVM-based VIP diagram blocks for LPDDR3 memory.

successful process is validated by the read operation given the input signals applied to the memory that is captured by a command monitor. The read data is captured by a data monitor and both monitors send their data to the analysis components. The scoreboard decides if the behavior is correct, and the coverage collector delivers the percentage of all possible cases of analysis. This process is repeated the number of times that the designer considers necessary to obtain a high percentage of coverage of all the possible cases of analysis.

*3) Simulation results:* Design analysis delivers successful results about the behavior of the design against the tests made. The design analysis is delivered by the scoreboard that shows a summary of the simulation results with all the design errors, warnings, fatal simulation errors and other data that can be specified to be plotted in the scoreboard. Fig.5 displays the UVM report summary of the LPDDR3 simulation. The number of operations can be observed along with other data such as a

TABLE II
LPDDR3 SIMULATION COVERAGE RESULTS.

| Item | | |
|---|---|---|
| Parameter | Description | Coverage (%) |
| Use of all banks in a sequence. | 8 used banks | 100 |
| Bank0 to Bank7 | Col | 100 |
| | Row | 100 |
| Total cells/bank | 16,777,216 cells | 5.96 |

total number of errors of the test, warnings and the total time of the simulation as well.

```
--- UVM Report Summary ---
** Report counts by severity
UVM_INFO : 66150003  UVM_WARNING : 0 UVM_ERROR : 0 UVM_FATAL : 0
** Report counts by id
[READING OPERATION ]  22050001  [WRITING OPERATION ]  22050001
[RNTST]   1  [SELF CHECKER]  22050001  [TEST_DONE]   1
Simulation complete via $finish(1) at  time 318499991250 PS + 50
```

Fig. 5. UVM report summary delivered at the end of the simulation.

Coverage analysis for this design shows that software limitations can avoid to obtain a total coverage in the simulation.The verified LPDDR3 memory is configured in 8 banks, each one has 1024 columns and 16,384 rows. The coverage collector samples all input variables applied to the LPDDR3 to show the data from Table II. The 100% of coverage is obtained in the analysis of rows and columns (not crossed) for all banks of the memory. However, a complete analysis might contain all memory cells for each bank. The maximum possible coverage for this item is just $5,96\%$ due to the limitation of software.

### B. A 3.3V Bandgap VIP

*1) Design:* A bandgap voltage reference is an analog circuit that provides a stable voltage reference which should be independent of voltage supply, process and temperature variations. Fig.6 shows the schematic of a bandgap reference circuit tested by the VIP system, delivering a typical reference voltage of 1.26V ($V_{REF}$). The output voltage must keep invariant as long as power supply changes. The verified circuit has a digital trimming port ($TRM$) to adjust output voltage.

*2) VIP system implementation for Bandgap:* Here, we highlight two VIP functions to test the bandgap circuit. First function generates different sequences varying $V_{DDA}$ such that different starting supply ramps are applied. The second function is the analysis of the output voltage of the bandgap against different supply stimuli. Fig.7 illustrates the diagram block of the bandgap VIP system where the two main operations are highlighted. In the test sequences, $V_{DDA}$ sequences are shown as start-up ramps with $\Delta t$ adjustable by the designer in order to analyze the starting speed of the bandgap circuit. This start-up ramps can be performed as a single ramp or as multiple and continuous ramps with different start-up times $\Delta t$. Ideal ramps also can be replaced by a starting signal with distortion. Fig.7 shows a start-up sequence with a ramp that has glitches. In addition, continuous ramps can be generated with different rise-and-fall times and different maximum-and-minimum voltage to analyze the behavior of the circuit due to

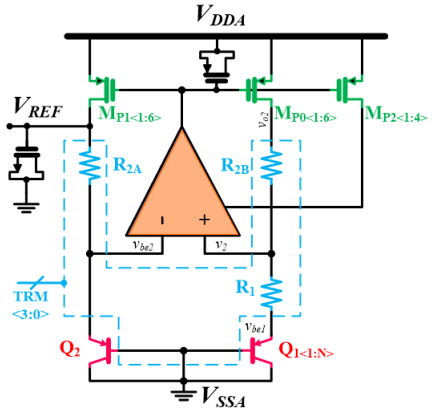


Fig. 6. Bandgap voltage reference schematic.

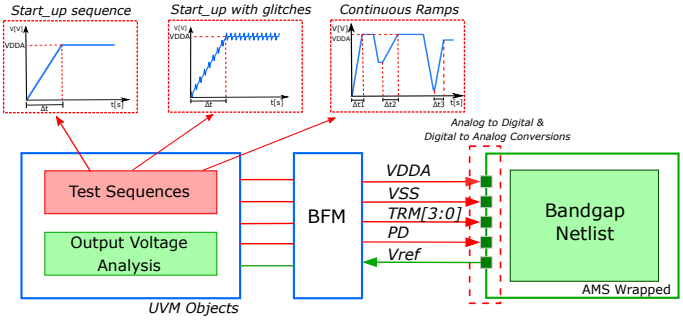


Fig. 7. Bandgap VIP diagram blocks.

supply variations through long intervals. The pass/fail criteria for $V_{REF}$ is based on a tolerance of 1% with respect to the designed reference voltage (1.26V), once the $V_{DDA}$ ramp exceeds this voltage.

*3) Simulation Results:* The sequences mentioned in the previous subsection are executed to obtain the results showed in this subsection. Table III presents the results of the start-up sequence, variating the rising time parameter in steps of 10 from $10\mu s$ to $100ms$, keeping remaining $V_{DDA}$ at its maximum value per $100us$. In this table, the $10\mu s$ and $10ms$ ramps show some failures which indicate that the circuit does not have enough speed to support these start-up times. Table IV shows the simulation results in the start-up sequence using glitches where these results are similar to the previous start-up results but with more flaws. Finally, applying continuous ramps, variating the rising and falling time (10-100,000$\mu$s) and $V_{DDA}$ maximum and minimum values ($1.5<V_{DDA}<3.3$ and $0.6<V_{DDA}<1.2$ respectively), successful simulation results were obtained, passing all tests performed.

## III. Analysis of Results

Here we discussed how successful was the verification process for each presented design in previous section, and by describing the UVM features that allowed to design a reliable verification system.

TABLE III
START-UP SIMULATION RESULTS IN SCHEMATIC (SCH) AND POST-LAYOUT (PSL) FOR THE BANDGAP.

| **Rising time [$\mu s$]** | **VDD [V]** | **Pass Sch / PsL** | **Fail Sch / PsL** |
|---|---|---|---|
| 10 | 0 <VDD< 3.3 | 623 / 749 | 380 / 254 |
| 100 | 0 <VDD< 3.3 | 900 / 728 | 103 / 275 |
| 1000 | 0 <VDD< 3.3 | 1003 / 1003 | 0 / 0 |
| 10,000 | 0 <VDD< 3.3 | 1003 / 1003 | 0 / 0 |
| 100,000 | 0 <VDD< 3.3 | 1003 / 1003 | 0 / 0 |

TABLE IV
START-UP WITH GLITCHES SIMULATION RESULTS IN SCHEMATIC (SCH) AND POST-LAYOUT (PSL) FOR THE BANDGAP.

| **Rising time [$\mu s$]** | **VDD [V]** | **Pass Sch / PsL** | **Fail Sch / PsL** |
|---|---|---|---|
| 10 | 0 <VDD< 3.3 | 605 / 721 | 398 / 282 |
| 100 | 0 <VDD< 3.3 | 872 / 708 | 131 / 295 |
| 1000 | 0 <VDD< 3.3 | 1003 / 1003 | 0 / 0 |
| 10,000 | 0 <VDD< 3.3 | 1003 / 1003 | 0 / 0 |
| 100,000 | 0 <VDD< 3.3 | 1003 / 1003 | 0 / 0 |

### A. LPDDR3 VIP

Limitations in the coverage analysis were observed after running simulations. In the case of the LPDDR3, it was not possible to analyze the total number of addresses per bank since the simulation software limited the analysis to 1 million cases in a single group of analysis of crosses, a cross being a certain row and column. Each memory bank has a total of 16,777,216 crosses, which exceeds the capacity of the commercially available tools.

It is common to claim that UVM reliability decreases as the design is more complex. Although UVM can perform a satisfactory verification regardless of the number of functions a system might have, the real problem of UVM for digital analysis arises when designs require to test all the possible cases of operation in order to prove correctness.

### B. Bandgap VIP

Bandgap VIP allows for exploration of different input conditions by applying sequences that are not possible to generate with tools in analog and mixed-signal domain. Bandgap simulation using UVM, compared to traditional analog simulations, different voltage sequences could be applied in order to make decisions about its correct operation automatically. Moreover, the VIP generates a report with all simulated cases presenting the possible failures. Although UVM does not replace an analog simulator, it does complement the types of analysis that must be done to ensure that a circuit is properly addressed.

Analog simulation results presented a considerable number of errors, but this does not indicate that the design works incorrectly. As shown in Fig. 8, the bandgap presented a certain percentage of error in certain tests. In a digital hardware test, obtaining a similar number of errors would mean a large failure in the logic of the circuit, while for an analog circuit it depends on the test that is being performed. Analog

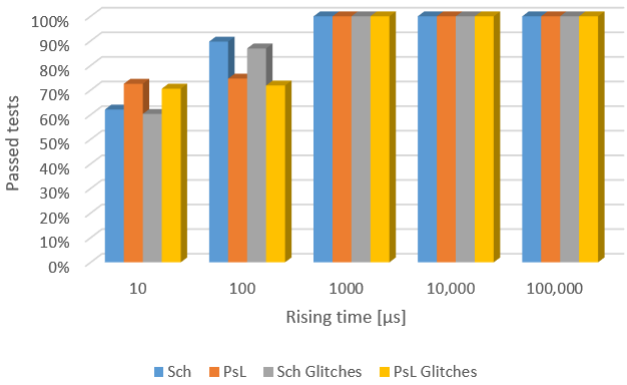


Fig. 8. Bandgap simulation results for start-up ramps tests.

simulations may require greater intervention on the part of the designer, since these simulations work with real values and the UVM analysis system may consider something as an error when, in fact, it is not critical. Furthermore, coverage gets impacted by the discrete steps used in simulation considering large run-time, which can be prohibitive when post-layout netlists are used.

Reliability of the bandgap simulation is only based on a behavioral level and not as a tool that ensures correct voltage or current measurements. Although UVM offers a great advantage by automating the simulation and performing analyzes that are not possible with a traditional analog simulator, its application is well fitted to test a circuit and compare it with a behavioral pattern given a certain tolerance.

## IV. SUMMARY

This paper presents an analysis of the reliability of UVM-AMS. Two different systems are tested in order to verify the reliability of the verification process, an LPDDR3 memory interface and a bandgap reference circuit. The LPDDR3 memory interface VIP presents successful results at a behavioral level but results were limited by software, which impacted the final coverage results. Although the bandgap VIP results showed advantages of implementing UVM to test analog circuits, verification reliability for this type of circuits is focused on a behavioral analysis rather than a measurement quantitative tool. The paper shows a UVM-AMS as a complement to the required test that must be performed on an analog circuit.

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