A Multi-Level Power-on Reset for Fine-Grained Power Management

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***Abstract*—Several proposals of power-on-reset (POR) circuits have been reported in the literature, however only a few number of them offer the possibility to have configurable reset voltage levels. This paper proposes a POR circuit with programmable voltage thresholds allowing to operate in a wide number of applications. The circuit is based on a multi-level voltage reference using native transistors, which allows to have a reduced area and power consumption. The POR is designed in a 0.18 μm standard-logic CMOS technology and occupies an area of 83μm x 68μm. Simulations results show a robust performance regarding temperature and process variations.**

***Index Terms*—Power-on Reset (POR), delay adjustable, multiple threshold, power-on detection, supply monitoring.**

I. Introduction

Fine-grain power management is required in energy-autonomous and battery supplied applications at the edge of Internet-of-Things. Power Management Units (PMU) power memory, digital core, peripheral and accelerators into idle and sleep states to save energy. Fig. 1 shows a PMU traditional scheme in a System-on-Chip (SoC); each supply voltage is commonly constrained to the lowest operational level of the block without impacting their robustness. Power supply is restored by re-enabling individual voltage regulators of each power gated block.

Although a power-up scheme to move from turned-off mode to active mode might be implemented for the entire SoC to alleviate load regulation, individual voltage supply networks might still suffer from local regulator settling time. Restoring supply from local regulators require a finite time to reach steady nominal voltage. During the ramp up of a local supply, memory and registers might have floating states causing undesired initial behavior [1]. In order to avoid floating states, a common solution is to hold the circuit into the reset state until local supply voltage reaches a level that guarantees correct operation. This task is done by a power-on reset (POR) circuit, which generates a reset signal during the supply transient state.

Traditional POR circuits are designed with a fixed threshold level detection forcing to place a different POR for each supply network [1]–[3]. Implementation of a single POR circuit for each voltage domain increases design area and cost considering its re-design to adjust the threshold level. This work presents a POR based on a multilevel voltage reference enabled to operate within the PMU without requiring multiple instances at the chip level. Proposed POR is capable to track supply ramps as fast as 1μs in a wider voltage range operation.

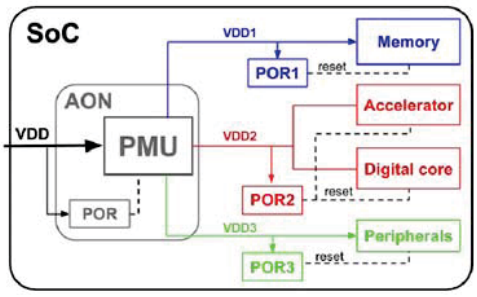

Fig. 1: SoC with multiple supply voltage domains.

II. Related Work

Several circuit topologies to generate a power-on reset signal have been reported in the literature. The most traditional way to implement the POR circuit is using a RC circuit as a delay cell and a comparator as a pulse generator [1] . Due to the large silicon area required to obtain an acceptable reset time (related to a large RC time constant), multiple techniques has been explored to replace the RC network. Circuits formed by series of diodes, summation of transistors's threshold voltages, and self-biased current sources has been implemented in on-chip applications looking for producing a delay in the reset signal [3] [4].

More complex architectures have been proposed in order to get zero static current, and in consequence low power consumption [2], [5]. These architectures also deal with ramp-up rate, temperature and threshold voltage variations, which are common issues that affect reliability of a POR circuit. However, all of the circuits mentioned above have fixed reset voltage thresholds whence their implementation in a multiple supply voltage system is not efficient.

A POR topology with low power consumption, configurable delay time, and a wide range of supply voltage operation is presented in [6]. The circuit consists on a modular architecture that can be implemented in series, enabling configurable delay times. The operation of the POR delay cell is based on the threshold operation of MOSFET transistor. The whole POR circuit is composed by ten modules and can operate for a voltage range of $1.8V < V_{DD} < 3.3V$ and a ramp of $100ns < t_{rise} < 1ms$. However, the circuit performance under temperature variations is not reported, which could be critical considering that the circuit is biased in sub-threshold region.

The POR circuit proposed in this work provides configurable delay time and reset voltage thresholds, keeping a low power consumption. These characteristics allow to use the POR in low power applications where power budget is at limit

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and the PMU turns on subsystems only when an operation demands.

III. Multilevel POR Circuit

A. Applications

Fine-grain power management generally adopts a PMU scheme as Fig. 1 shows. That kind of scheme aims to efficiently supply every sub-system where different voltage domains can be found. One example of multiple voltage domains is shown in Fig. 2, considering PMU should be always on in order to administrate power gating of all other domain. Activation of local regulators is provided by PMU and the POR ensures a safe start up in every domain.

A power management scheme, such as presented in Fig. 1, can be used in IoT device which are battery powered or even powered by energy harvesting systems. Power efficiency in those scenarios is a critical issue due to target applications need extended battery life. Longer battery life implies reduction and reuse of most of resources avoiding unnecessary power consumption. A possible option of power optimization is reduce all PORs circuits to only one. In that case, an additional Mux is required to select the supply voltage that has to be monitored.

Requirements in a PMU with only one POR circuit imply multiple operation levels. A POR circuit that can be triggered with different voltage levels could simply provide the start up of every domain by a re-configuration through the PMU. Considering PMU is always on, required configuration for POR circuit can be provided every time a sub-system need to be powered on. PMU plus POR with multiple trigger level is not only power efficient but also area efficient due to only one circuit is required.

Further applications for a Multi-level POR can be found if a harvesting system is considered. Zero battery charge implies harvesting system is working to supply a device. In that condition, no additional power consumption is desired, making useful to power off even the PMU. Generally, a near threshold voltage logic is implemented for low power operations, logic that can be turned on using the lowest voltage level of multi-level POR. Low voltage logic can configure a new POR trigger level, preparing it for switching on PMU when harvesting system achieve a higher supply level.

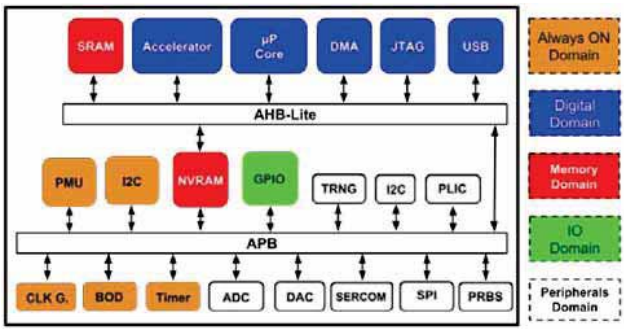

Fig. 2: Microarchitecture details of the SoC with clearly identified voltage domains.

B. Proposed circuit description

The proposed POR is composed by three functional blocks as shown Fig.3. The first block is a voltage reference with an adjustable output allowing to generate a multiple range of voltage for the reset point. The second block is a voltage detector that follows the supply voltage V_{DD} and generates a delayed signal for the pulse generator. The pulse generator switch when the detected signal crosses its threshold voltage. Optionally, a counter can be added to provide the possibility of controlling the reset time if the system needs a longer time to establish its normal operation.

The voltage reference is based on the low power sub-threshold reference source proposed in [7]. The circuit consists on a zero-V_{th} native NMOS device *MN*, followed by a group of four stacked PMOS transistors (*M1,M2,M3,M4*) connected as diodes. The native transistors has a Complementary to Absolute Temperature (CTAT) behavior, while each PMOS has a Proportional to Absolute Temperature (PTAT) characteristic. A low temperature coefficient is achieved when the CTAT current acts as the bias source for the PTAT devices.

When process variations results in a slow-slow corner, leakage current of PMOS transistors is comparable to the sub-threshold current at low-temperature, degrading the performance and thus requiring an additional compensation. To enhance the temperature coefficient it is necessary to increase the current of the PMOS stack. This task can be done by switching MN_x native transistors through the TRIM signal. As a consequence, *MN* together with MN_x act as an effective wider transistor, enlarging the current flowing through the PMOS devices and improving the temperature coefficient. It is important to highlight that extra compensation becomes harder when the PMOS stack is increased (when generating four or more reset levels) because static current drops dramatically.

Various considerations must taken into account to select an optimal topology for a voltage detector circuit. It is expected that the POR circuit will be integrated in the same die as the main digital circuit. For that reason, voltage detector may occupy very reduced silicon area and provide enough delay time to guarantee that the supply voltage reaches an enough value for the correct function of digital cells. In order to accomplish this requirements, the designed voltage detector use the concept of an RC network composed by the capacitor C and the resistor R2.

At the beginning of operation, the supply voltage V_{DD} is too low and the transistor M5 remains off and the capacitor is discharged. As a consequence, a zero logic is established at the input of the pulse generator, setting the *RESET* signal in active mode. When V_{DD} is rising up, transistor M5 is turning on, generating a current and gradually charging the capacitor C. This charge time depends on the slope of the V_{DD} ramp and is controlled by the difference between the current supplied by M5 and the current sinked thorough the branch conformed by R2 and M6. The time that the *RESET* signal is held in active

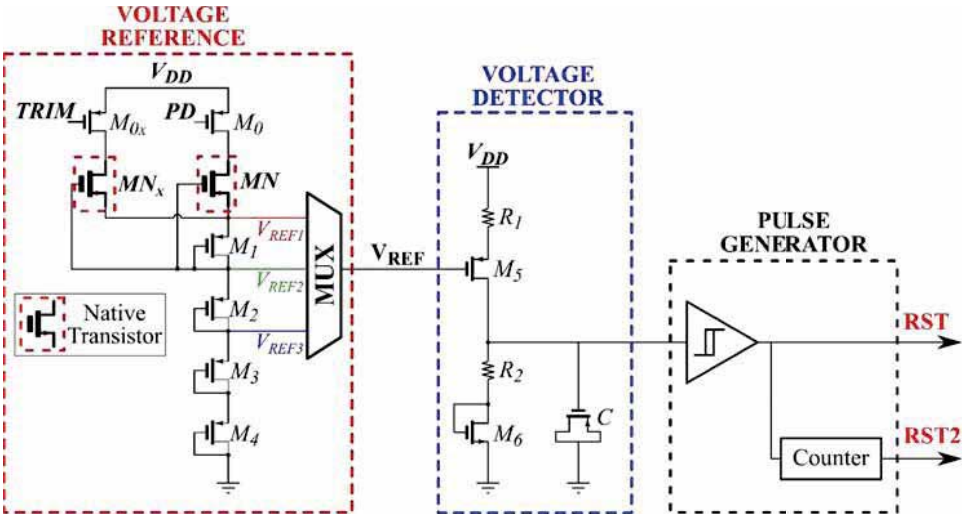

Fig. 3: Proposed POR circuit.

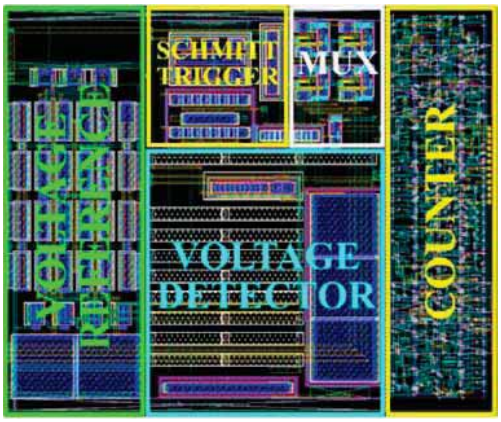

Fig. 4: Layout of the POR Proposed.

mode depends of the charge time of the capacitor and the established high threshold voltage of the Schmitt-Trigger.

Once the supply voltage reaches the set level it is possible to use the Schmitt-Trigger's output to enable a counter. This configuration offers the ability to have different reset times, according to a particular application requirements. Thus, the selection of *RESET* or *RESET2* as the system reset can be configured, making the reset time independent of the chosen voltage level.

IV. Results

The POR circuit was implemented in a TSMC $0.18\mu m$ CMOS technology, occupying an area of $83\mu m$ x $68\mu m$. The nominal power supply is 3.3V, which corresponds to the I/O value of the used technology. Fig. 4 shows the layout of the proposed circuit. This section discusses the test benches used for circuit validation as well as the obtained results. Finally, the performance of the proposed POR is compared with state-of-art POR circuits.

During the chip power-up, the supply signal ramp could have different rising times, according with physical and factory characteristics of the battery. For this reason, in order to test correctly the POR circuit, several rising-times for VDD ramps between $1\mu s$ and 50ms were employed in post-layout simulations. Fig. 5 shows the output reset pulse for three different threshold levels, and considering a supply ramp of 50ms. As it can be seen, the POR circuit responds correctly for the three trigger levels set by the selected V_{REF}. The first reset signal goes to high when supply voltage is 0.79V, while the second and third reset are deactivated when supply is 1.77V and 2.22V respectively.

The peak that occurs at the beginning of the powering-up is due to the time necessary to load the parasitic capacitances of the Schmitt trigger transistors. This peak is not relevant because its value does not even reach the threshold voltage of transistors, which is around 700mV. The pulse that occurs when the reset signal goes up can be used as an enable for the counter. This feature is useful when circuits such as oscillators and clocking circuits require a long reset-time.

Fig. 6 shows the simulation results for the same test but for a V_{DD} ramp of $1\mu s$; PVT variations were included as well. The circuit generates an effective POR signal in all corners. Also, the three thresholds levels fixed by the voltage reference can be distinguished. Multiple thresholds give the possibility of select the POR trigger voltage level in applications that integrates a PMU and implements different voltage supply.

In case of a 50ms V_{DD} ramp, the MOSFET capacitor is charged with a lesser voltage than when considering a quick V_{DD} ramp. It makes that when the low threshold level is selected and when considering high temperature and fast PMOS process corners, the circuit does not generates a POR signal. In consequence, the reset signal follows the supply ramp as is shown in Fig.7. It is important to note that this this behavior only limits the implementation whit ramps slower than 50ms.

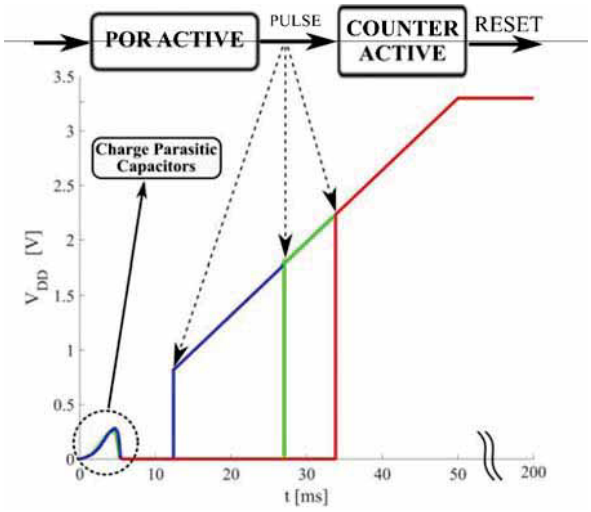

Fig. 5: POR Signal for a V_{DD} ramp of 50ms.

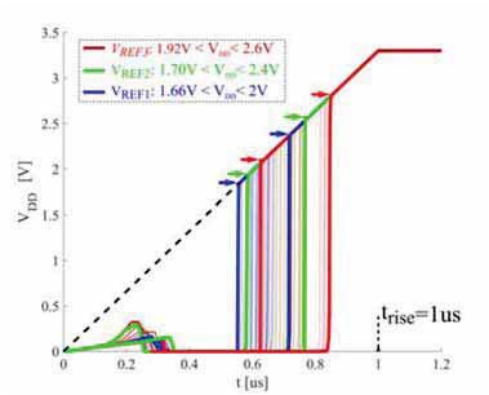

Fig. 6: POR signals corners case without trimming for V_{DD} ramp of 1us.

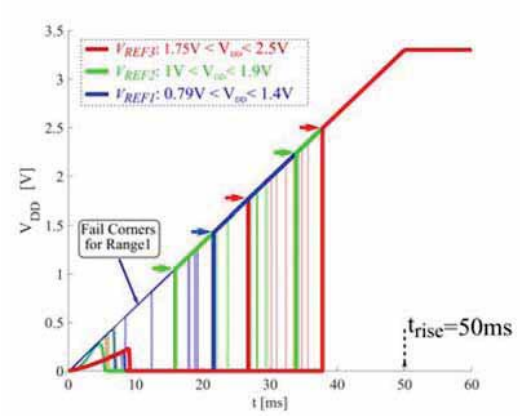

Fig. 7: POR Signals corners case without trimming for a V_{DD} ramp of 50ms.

Table I shows the performance summary. The circuit was validated for the industry temperature range (from -40°C to 120°C) and for all process corners. The POR offers three different reset voltage thresholds over 1V according with the chosen V_{REF}. The current consumption is shown for two different cases: when the voltage is in steady state and the POR continues operating i.e. static behavior; and when the POR is power down, implying that the circuit is used only to provide the reset during load regulation. Static current is 7μA with a maximum variation of 4μA; and Power-down current is always lower than 640nA. Finally, Table II compare the performance of the proposed POR with state-of-art topologies.

		Reset Threshold [V].					
		Min.		Typ.		Max.	
VDD Ramp		1us	50ms	1us	50ms	1us	50ms
Range1		1.66	-	1.85	0.79	2	1.41
Range2		1.7	1	2.19	1.77	2.4	1.92
Range3		1.92	1.75	2.25	2.22	2.6	2.48
Current Consumption	Static [uA]	5		7		11	
	POR off current [nA]	0.16		9.55		640	

TABLE I: POR Results Summary

Ref.	Quiescent Current [uA]	Power-on Rising Time [ms]	Supply Voltage Range [V]	Threshold Level Adjustable	Technology[um]/ Area [um^2]
[6]	0.076	<10	1.2 - 3.3	Yes	0.5/1900
[5]	0	<1	1.8 - 5.5	No	0.5/27000
[1]	1	1000	1.8	No	0.18/12000
This work	7	<50	1 - 3.3	Yes	0.18/5700

TABLE II: POR Comparison Summary

V. Summary

In this paper a POR circuit with configurable voltage levels and delay reset is presented. A temperature compensated sub-threshold voltage source is employed to generate the voltage references required for the circuit. Simulation results over PVT variations, show a robust performance within the industrial temperature range from -40°C to 125°C, with a maximum current consumption of 11μA in the worst-case, and enabling up to 3 different POR levels for different SoC applications. In spite of the the current consumption is larger compared with the state-of-art, the circuit is attractive due to its configurability and small area.

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