On-Fly Offset-Correction Method for High-Speed Comparators using All-Digital Phase Measurement

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***Abstract*—This paper presents a low-cost technique to reduce offset voltage of a dynamic comparator. The proposed method is based on output-data phase measuring through a digital implementation without impacting offset accuracy. The technique requires less than 500ns to achieve convergence and calibration without needing to break the signal path associated to the comparator during regular link operation. An on-a-chip emulated channel and front-end with a sampling circuit has been implemented in 130nm CMOS along with a chip-scope capability to measure eye diagrams at the input of the sampler. Although the concept has been implemented in a low speed interface considering available technology, the implementation shows potential to port the proposed offset correction scheme to a state-of-the art process node applied to links featuring data rates with tens of Gb/s.**

***Index Terms*—Offset correction, digital calibration, voltage comparator.**

I. Introduction

OFFSET reduction technique is one of the major concerns at the front-end of a high-speed wireline receiver considering the additional complexity and load penalty to the signal path. Comparators in current links face the challenge to sample signals at data rates above 20Gb/s with amplitude signals as low as 20mV considering the aggregated losses up to 40dB in channels [1]. As a result, comparator sensitivity specifications become limited by the accuracy of the offset correction scheme, which at the same time, the implemented scheme must not load the signal path such as the signal amplitude get impacted.

Several works have been reported [2]–[5] which include the usage of back-end digital algorithms that increases complexity and/or circuit techniques that add loading to the signal path. In all cases, it is necessary to make calibration including an additional signal path to avoid breaking the link. It means, while circuitry on the first path is processing information, the additional path is making the calibration process.

In this work, a novel scheme for reducing offset of dynamic comparators used in high speed interfaces is presented. The proposed scheme has been fabricated and measurement results show its potential application at on-fly offset correction in high-speed link receivers. The technique is based on the output signal phase and presents low complexity and fully digital implementation for the calibration circuitry without compromising speed and load. In addition, this approach can calibrate the comparator without interrupting the transmission process paving the way to eliminate the implementation of the alternative signal path in case adaptation paths are not required.

II. Proposed Offset Reduction Technique

The proposed technique is based on sensing offset through the output phase of the dynamic comparator. This offset measurement is provided by a phase detector, whose output controls the transition of a Finite-State-Machine (FSM) and thus the bias current of a preamplifier, as shown in Fig. 1. The correct adjustment of this currents will reduce the total offset, including extra offset added by the preamplifier.

The Fig. 2 illustrates the behavior of the technique: assuming an offset with the enough amplitude to saturate the comparator —so that making impossible to differentiate between a logic one or zero at the input— the output V_{o1} is clamped to V_{DD}, and V_{o2} is oscillating between V_{DD} and ground because the comparator is changing from reset to comparison phase as region A in Fig. 2 shows. While this condition is maintained, the UP signal at the phase detector (PD) output is always high, producing a differential increment of the finite-state machine (FSM) outputs and therefore causing steps increments in the differential bias currents I_1 and I_2. The change in the bias currents produces an additional offset V_{CORR} with the opposite polarity regarding $V_{\text{off1}} + V_{\text{off2}}$. With $V_{\text{CORR}} = -(V_{\text{off1}} + V_{\text{off2}})$, the output V_{o1} of the comparator would go low when the next logic zero reaches the input (region B of Fig. 2). In the next rise edge of V_{o1} the phase detector resets and finishes the increment process at the currents with finally exchanging V_{o1} and V_{o2} roles (region C). Thus, the process can be restarted in the opposite direction, making the currents to be oscillating around the new reached DC level. These final

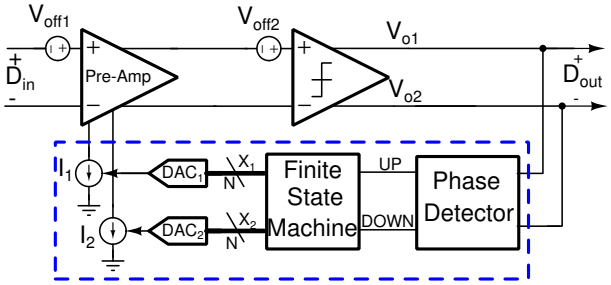

Fig. 1: Block diagram of the proposed offset reduction technique.

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currents condition can be used as a stop criterion of the calibration process.

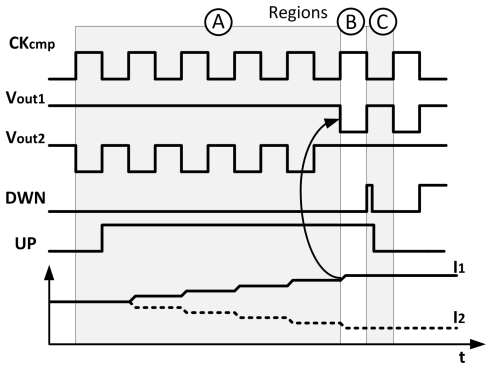

Fig. 2: Timing diagram of the offset-reduction technique.

The implemented circuits used in the control loop of the calibration process are described as follows: the PD structure is shown in Fig. 3, which consists of two D-type flip-flops and a NAND gate at the output, that is, a classical frequency-phase detector used as PD. The FSM basically corresponds to two 8 bits UP/DOWN counters, which varies the X_1 and X_2 outputs words differentially. Finally, these words control the two DACs.

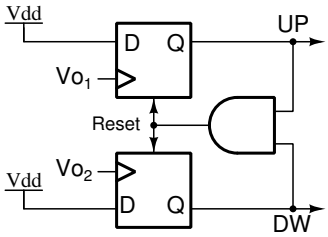

Fig. 3: Phase and frequency detector.

Traditional calibration techniques require to perform offset correction in at least two phases; interrupting the functional operation of the interface while the correction is done. In contrast, the calibration technique presented here allows to perform the correction while the whole interface is working.

Considering that calibration procedure is fully digital, PVT variations and mismatch of the additional circuitry —including mismatch of the two current sources— have a little effect on the performance. Moreover, the required time to complete the calibration is limited basically by the DAC settling. If high-speed converters are used, the calibration process can finish in less than 100 clock cycles.

III. Implementation and Experimental Results

A. Measurement Strategy

The proposed offset-reduction technique was tested according to the system shown in Fig. 4, which is composed by a programmable PRBS generator, a digitally-programmable low-pass filter, a digitally controlled phase-mixer, a strong-arm comparator with a current-controlled pre-amplifier, and a

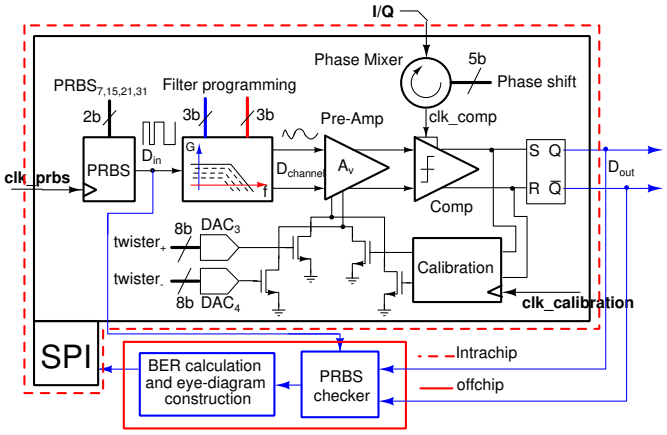

Fig. 4: System implemented for offset-reduction technique validation

SPI interface to set the scheme. The PRBS acts as a data generator with the purpose of emulating information from a communication link; the low-pass filter emulates a lossy-channel, and its programmable cut frequency is used to simulate different channel loss (bandwidth and attenuation). The phase mixer varies the sampling time at which the comparator senses the input data and the pre-amplifier has four different current sources: two are controlled by the calibration DACs, and the others two are used to introduce additional offset. Fig. 5 presents the layout of the implemented system, which was taped-out in a CMOS 130nm standard technology with V_{DD}=1.2V.

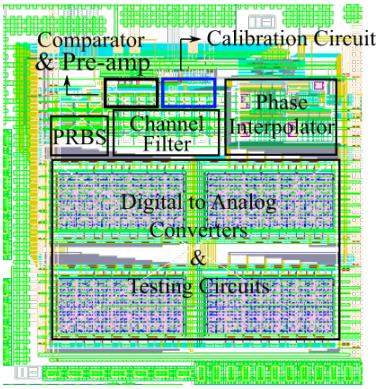

Fig. 5: Layout of the circuit that includes the proposed offset-correction technique.

The strategy to test the technique is to build an eye-diagram before and after calibration for the pre-amplifier input nodes, using comparator output-data collected through the SPI. The differences in apertures of the eye-diagrams show the effectiveness of the proposed method.

The eye-diagram can be constructed as follows: the comparator provides an unique comparison level and sampling instant, that if if the phase of the clock that controls the comparator is shifted in relation to the clock of the PRBS —through the phase mixer—, it is possible to sample the eye-diagram at different X-axis levels (time), as Fig. 6 shows. In

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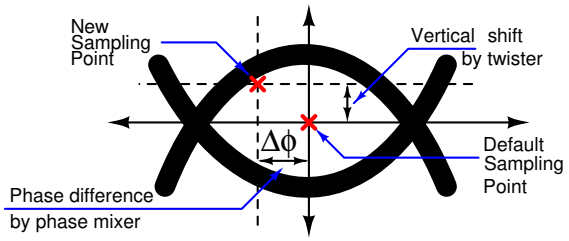

Fig. 6: Conceptual diagram of phase and voltage shifting to build the eye-diagram at the pre-amplifier input.

this way, when the BER is higher to 10^{-7} the comparator is sampling at a time (phase difference) in which the eye-diagram is open. Otherwise, if the BER is lower, the sampling instant corresponds to a closed region of the eye.

Aiming to sample the eye-diagram at diverse Y-axis levels (amplitude), the system introduce additional offset —through twister current sources of the pre-amplifier— whose effect is to shift the eye-diagram vertically. Therefore, the comparison level varies according to the twister's value. By continuously checking the BER, it is possible to know if the observation (comparison) point corresponds to an open/close eye-diagram region.

Finally, combining X-axis (time) and Y-axis (amplitude) displacements it is possible to build a complete eye-diagram without the need to access physically the pre-amplifier input nodes.

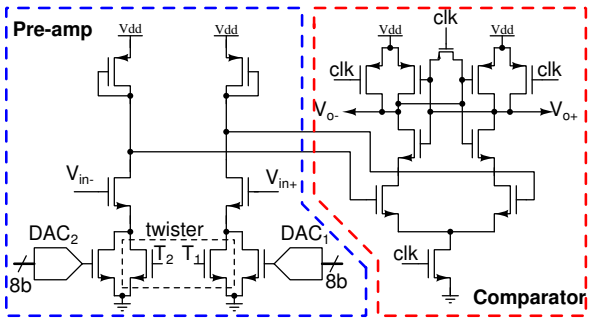

Fig. 7: Implemented sampling circuitry.

B. Implementation

Taking into account that the main idea of this paper is to show the performance of the proposed offset-reduction technique in a traditional receiver-end, the implementation of each building block of the scheme at Figs. 1 and 4 is based on classic structures as follows: the dynamic voltage comparator corresponds to the strong-arm topology; the pre-amplifier is based on a degenerated common-source circuit (Fig. 7); the PRBS corresponds to a shift-register counter with programmable word length; the low-pass filter is based on the Gm-C topology, using Nauta amplifiers; the phase mixer is implemented by the well known analog phase interpolator topology that uses in-phase and quadrature input clock signals provided by local PLL [6]; and the DACs corresponds to a

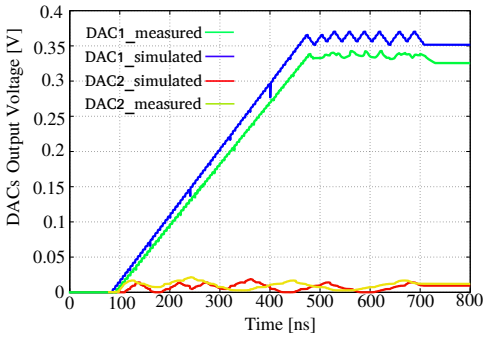

Fig. 8: Measured and simulated (TT) output voltage of calibration DACs during a calibration process.

classical R-2R topology. Finally, all the system was taped-out using a general purpose TSMC 130nm CMOS technology.

Considering that the phase-detector is connected directly to the output of the comparator, the additional load imposed by the flip-flops (Fig. 3) could be critical in high-speed applications. In this type of circuits the comparator is implemented in a Decision-Feedback-Equalizer (DFE) structure, in which the 1-tap and 2-tap need to be resolved within 1UI. Although additional loading could degrade timing performance, a traditional 18T-flop only adds a load equivalent to 1X fanout four inverter.

C. Experimental Results

Fig. 8 shows the simulated and measured DACs output signals while a calibration process is carried out. An offset voltage of 50mV is provoked by the twister transistors, which need to be compensated by the calibration circuit. DACs output signals reach the steady state after 400ns, indicating that the calibration process has finished. Although Fig. 8 shows the results for the typical-case simulation and measurements for one sample, the difference of 35mV between both signals indicates the influence of mismatch on the circuit. It is important to highlight that the calibration time could be reduced implementing a faster DAC.

Fig. 9 shows the eye-diagram at the input of the pre-amplifier without applying the calibration method, and using the procedure described in section III-A. The input data corresponds to a $PRBS_{11}$ source, a PRBS checker indicates the open/close region of the eye-diagram: if the BER is greater than 10^{-7} corresponds to a blue square of Fig. 9 (open region), otherwise refers to a red square (closed region). The vertical amplitude is 65.6mV and 132mV for a filter attenuation of 21dB and 14dB respectively, while the time window is 2.5ns —indicating a data-rate of 400Mb/s—. This diagram was constructed with a 5bit time (phase difference) resolution —which is related to the resolution of the phase mixer—, and 8b for amplitude shifts —DACs resolution—. These values imposes a step of 78ps and 4.6mV for X-axis and Y-axis respectively.

The measured offset is about 8mV for the eye-diagram of Fig. 9a, and 24mV for Fig. 9b; these values were calculated based on the difference between the maximum and minimum

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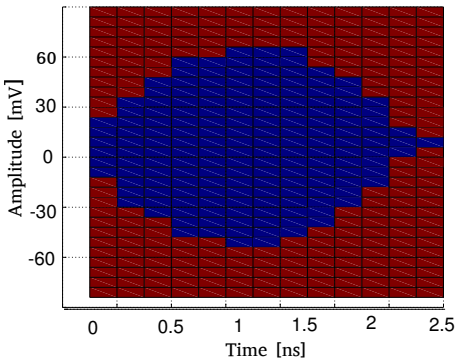
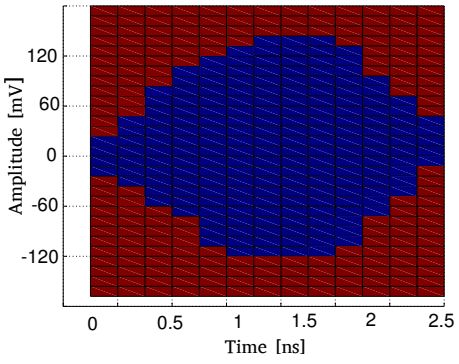
values of each diagram. This offset includes contributions of the pre-amplifier, the comparator and the twister's DACs. Fig. 10 shows the eye-diagram after calibration when filter attenuation is 14dB. The diagram is now centered around 0V, showing the effectiveness of the proposed technique. The residual offset is 4mV, which is caused mainly by the DAC resolution.

Another experiment was carried out in order to find the maximum unbalance that the circuit can compensate. It is analogue to displace the eye-diagram vertically, and find out the maximum displacement that the calibration circuit can reduce. A large unbalance measured in Fig. 9a and 9b is induced by the twister, then the calibration circuit is turned on and the BER is evaluated; next, the unbalance is increased even more and the calibration is carried out again as well as the BER calculation. The region in white of Fig. 11 shows that the eye-diagram of Fig. 9 can be moved up to 245mV resulting in a successful offset correction.



(a)



(b)

Fig. 9: Measured on-chip eye diagram before calibration: a) with 21dB of attenuation, b) with 14dB of attenuation.

IV. Summary

In this paper, a low hardware-overhead calibration technique for dynamic voltage comparators has been proposed and verified experimentally. The proposed technique uses phase as a variable to measure offset, and adjust a pre-amplifier bias current to reduce it. Experimental results show an offset compensation capability of 245mV, without degrading the

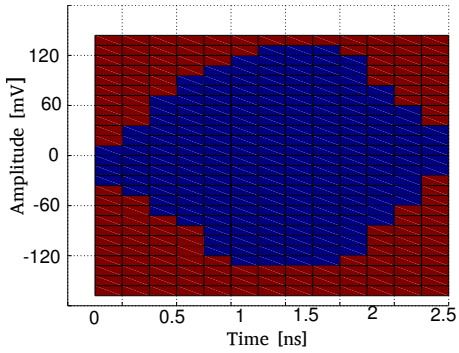


Fig. 10: Measured on-chip eye diagram after calibration.

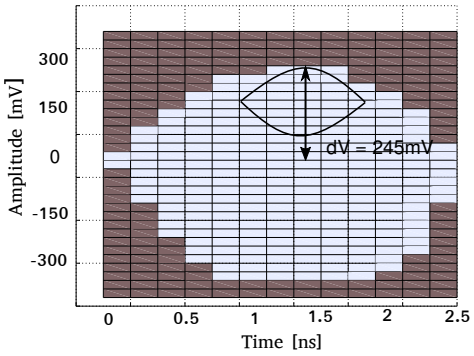


Fig. 11: Maximum unbalance range that the calibration can compensate.

communication system performance. The technique can be performed even during link-training procedures because it can use the initial bit-stream as data. Furthermore, the method tracks temperature and supply voltage variations influence over offset along data transfer. Finally, all the calibration circuit was fully synthesized, which allow to extend the technique to different fabrication process and applications. *A demo is available and can be presented it at the conference.

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